ICOM

SERVICE MANUAL

HF/VHF TRANSCEIVER

IC-706MKII

Icom Inc.

INTRODUCTION

This service manual describes the latest service information for the **IC-706MK Ⅱ** HF/VHF TRANSCEIVER at the time of publication.

VERSION NO.	VERSION	SYMBOL
#02	Europe	EUR
#03	France	FRA
#04	Denmark	DEN
#05	U.S.A.	USA

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 16 V. This will ruin the transceiver.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1110004080	S.IC	µPC2709T	IC-706MK Ⅱ	MAIN UNIT	5 pieces
8810009020	Screw	FH M2.6 x 5 ZK	IC-706MK Ⅱ	Top cover	10 pieces

Addresses are provided on the inside back cover for your convenience.

REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 50 dB to 60 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

TABLE OF CONTENTS

SECTION 1 SPECIFICATIONS

■ GENERAL

• Frequency coverage :

Receive	0.030 – 200.000 MHz*
Transmit	1.800 – 1.999 MHz*
	3.500 – 3.999 MHz*
	7.000 – 7.300 MHz*
	10.100 – 10.150 MHz
	14.000 – 14.350 MHz
	18.068 – 18.168 MHz
	21.000 – 21.450 MHz
	24.890 – 24.990 MHz
	28.000 – 29.700 MHz
	50.000 – 54.000 MHz*
	144.000 – 148.000 MHz*

*Depending on version.

• Mode : USB, LSB, CW, RTTY (FSK), AM, FM, WFM (WFM is for receiver only)

• Number of memory ch. : 102 (99 regular, 2 scan edges,1 call)

• Antenna connector : SO-239×2 (for HF/50 MHz and 144 MHz)/50 Ω

• Power supply requirement : 13.8 V DC ±15% (negative ground)

• Frequency stability : Less than ± 7 ppm from 1 min. to 60 min. after power ON. After that, rate of stability less than ±1 ppm/hr. at +25°C (+77°F). Temperature fluctuations 0°C to +50°C (+32°F to +122°F) less than ± 5 ppm.

• Current consumption :

Transmit	max. power	20 A
Receive	standby	1.8 A
	max. audio	2.0 A

• Usable temperature range : –10°C to +60°C (+14°F to +140°F)

• Dimensions : 167(W) × 58(H) × 200(D) mm
$6^{9}/_{16}$(W) × $2^{9}/_{32}$(H) × $7^{7}/_{8}$(D) inch

• Weight : 2.45 kg (5 lb 6 oz)

• CI-V connector : 2-conductor 3.5 (d) mm ($^{1}/_{8}$")/8 Ω

• ACC connector : 13-pin

■ TRANSMITTER

• Output power :

1.8–50 MHz band	SSB/CW/RTTY/FM	5–100 W
	AM	2–40 W
144 MHz band	SSB/CW/RTTY/FM	2–20 W
	AM	2–8 W

• Modulation system :

SSB	Balanced modulation
AM	Low level modulation
FM	Variable reactance modulation

• Spurious emissions : Less than –50 dB (HF)
Less than –60 dB (50, 144 MHz)

• Carrier suppression : More than 40 dB

• Unwanted sideband supp. : More than 50 dB

• Microphone connector : 8-pin modular jack (600 Ω)

• KEY connector : 3-conductor 6.35 (d) mm ($^{1}/_{4}$")

• RTTY connector : 3-conductor 3.5 (d) mm ($^{1}/_{8}$")

■ RECEIVER

• Receive system :

SSB/CW/AM/WFM	Double superheterodyne
FM	Triple superheterodyne

• Intermediate frequencies :

MODE	1st	2nd	3rd
SSB/FM	69.0115 MHz	9.0115 MHz	455 kHz*
AM/FM-N	69.0100 MHz	9.0100 MHz	455 kHz*
CW	69.0106 MHz	9.0106 MHz	—
RTTY	69.0105 MHz	9.0105 MHz	—
WFM	70.7000 MHz	10.7000 MHz	—

*FM or FM-N mode only

• Receive sensitivity : (pre-amp ON)

FREQUENCY	SSB/CW	AM	FM
0.5 – 1.8 MHz	—	13 µV	—
1.8 – 28 MHz*	0.15 µV	2 µV	—
28 – 29.999 MHz	0.15 µV	2 µV	0.5 µV
50 MHz band	0.12 µV	1 µV	0.25 µV
144 MHz band	0.11 µV	1 µV	0.18 µV

Note: SSB, CW and AM modes are measured at 10 dB S/N; FM mode at 12 dB SINAD.

*Except 4–4.5 MHz, 8–9 MHz.

• Squelch Sensitivity : (pre-amp ON)

SSB	Less than 5.6 µV
FM	Less than 0.32 µV

• Selectivity* :

SSB, CW, RTTY	More than 2.4 kHz/–6 dB
	Less than 4.8 kHz/–60 dB
AM/FM-N	More than 8.0 kHz/–6 dB
	Less than 30 kHz/–40 dB
FM	More than 12 kHz/–6 dB
	Less than 30 kHz/–60 dB

*Without an optional filter unit and with mid bandwidth selected.

• Spurious and image rejection ratio:
70 dB (except IF through/50 MHz)
60 dB (144 MHz FM mode)

• Audio output power (at 13.8 V DC) : More than 2.0 W at 10% distortion with an 8 Ω load

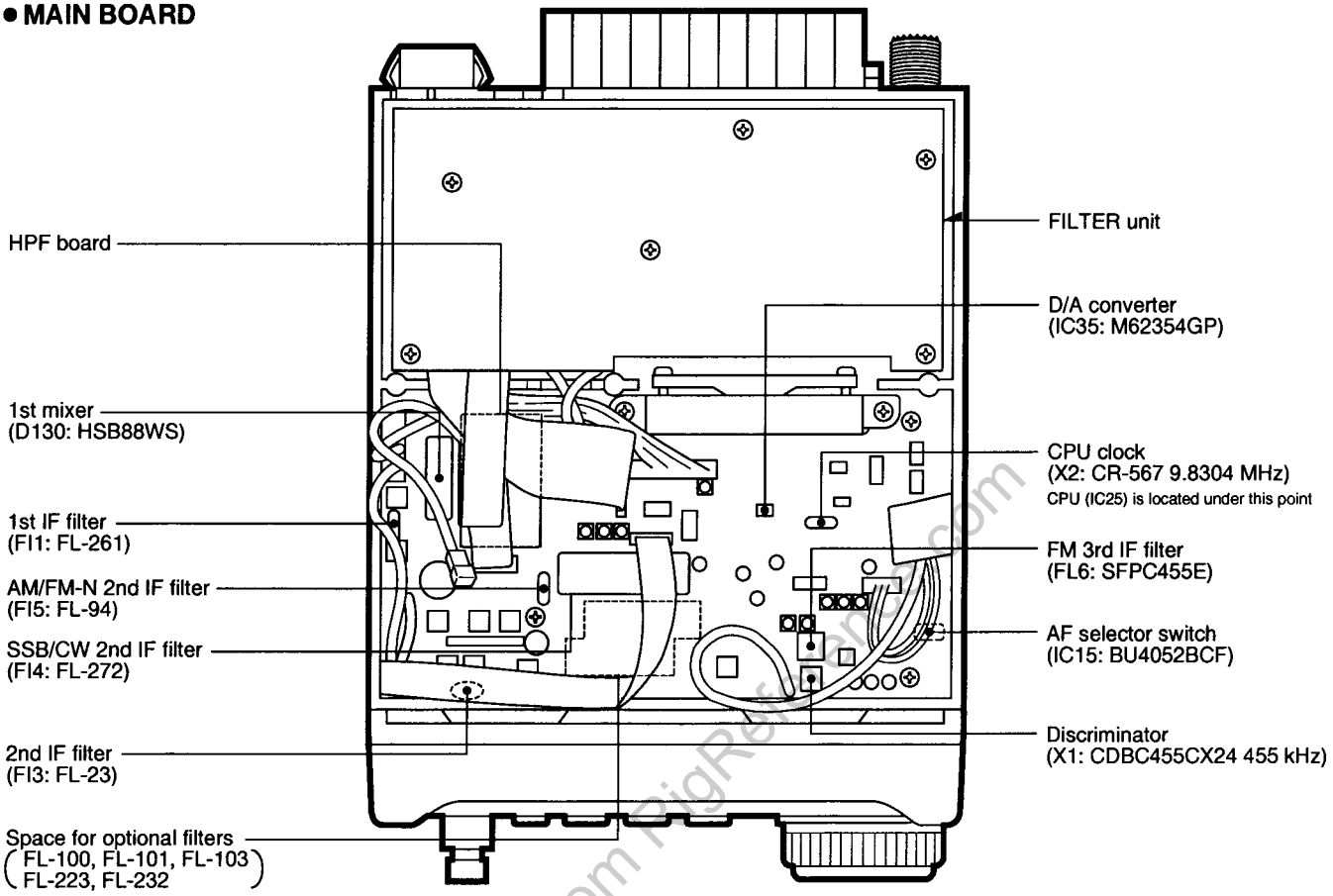
• RIT variable range : ± 9.99 kHz

• PHONES connector : 3-conductor 3.5 (d) mm ($^{1}/_{8}$")/8 Ω

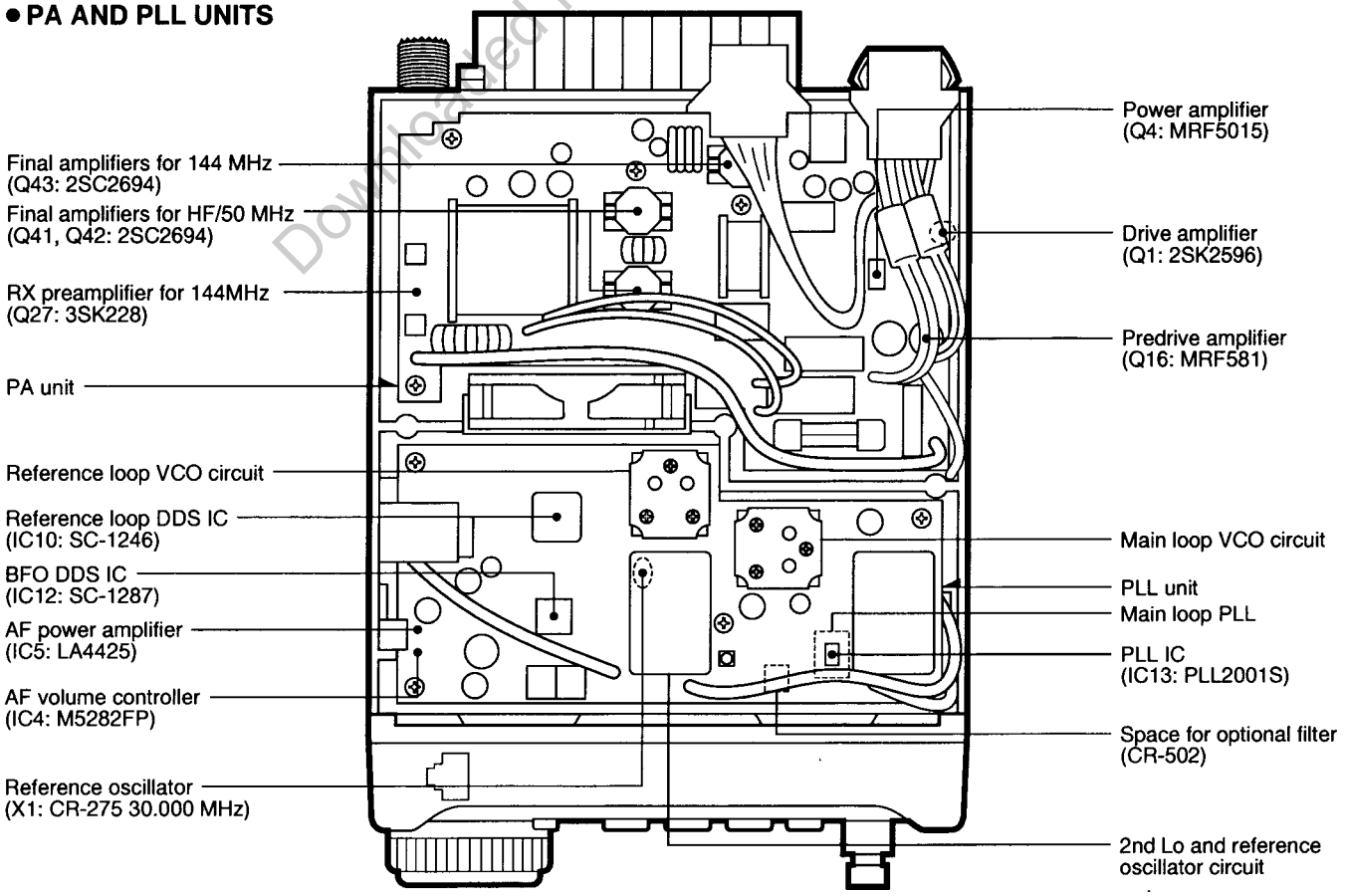
• EXT SP connector : 2-conductor 3.5 (d) mm ($^{1}/_{8}$")/8 Ω

SECTION 2 INSIDE VIEWS

● MAIN BOARD



● PA AND PLL UNITS



SECTION 3 CIRCUIT DESCRIPTION

3-1 RECEIVER CIRCUITS

3-1-1 HF/50 MHz RF CIRCUIT (FILTER, MAIN AND HPF BOARDS)

HF/50 MHz RF filters pass only the desired band signals and suppress any undesired band signals. The HF/50 MHz RF circuit has 7 low-pass filters and 6 high-pass filters for specified band use.

HF/50 MHz RF signals from the [ANT1] connector, pass through one of 7 low-pass filters as below, the transmit/receive switching relay (FILTER unit; RL1) and low-pass filter (FILTER unit; L1, L2, C1–C5), and are then applied to the MAIN board via J1 (FILTER unit).

• Used RF low-pass filter (FILTER board)

Band	Control signal	Input relay	Band [MHz]	Control signal	Input relay
0.03–2 MHz	L1	RL15	15–22 MHz	L5	RL11
2–4 MHz	L2	RL13	22–30 MHz	L6	RL7
4–8 MHz	L3	RL5	30–60 MHz	L7	RL3
8–15 MHz	L4	RL9			

The signals from the FILTER board are applied to or bypass the 20 dB attenuator (R3, R4). The signals pass through the high-pass filter (L3, L4, C3–C7) to suppress strong signals below 1.6 MHz and are then applied to the HPF board via the "TOAT" terminal.

(1) 0.03–2 MHz and 30–40 MHz

The signals pass through a low-pass filter (L23, L24, C38–C42), and then applied to the preamplifier circuit on the MAIN board.

(2) 2–30 MHz

The signals from the low-pass filter (L23, L24, C38–C42) are applied to one of 6 high-pass filters as at right above and are then applied to the preamplifier circuit on the MAIN board.

(3) 40–60 MHz

The signals pass through the low-pass filter (L25, L26, C43–C46, C60) and the high-pass filter (L29, L30, C47–C51) via D13 and are then applied to the preamplifier circuit on the MAIN board.

• Used RF high-pass filter (HPF board)

Band	Control signal	SW diode	Band [MHz]	Control signal	SW diode
0.03–2 MHz	TH	D5	15–22 MHz	H5	D21
2–4 MHz	H2	D16	22–30 MHz	H6	D7
4–8 MHz	H3	D20	30–40 MHz	TH	D5
8–15 MHz	H4	D17	40–60 MHz	BV, T8	D13

3-1-2 VHF RF CIRCUIT (PA UNIT)

The VHF RF circuit passes and amplifies only the desired band signals and suppresses any undesired band signals. The VHF RF circuit has a preamplifier and 2 bandpass filters.

The VHF RF signals from the [ANT2] connector pass through the low-pass filter (L16, L17, C35–C39) and antenna switching circuit (D4, D14, D15, D24). The signals are amplified at the preamplifier circuit (Q27) between the 2 bandpass filters (D21, D33 and D19, D31).

The filtered signals are applied to the MAIN board via J12 (PA unit) and are then applied to the preamplifier circuit.

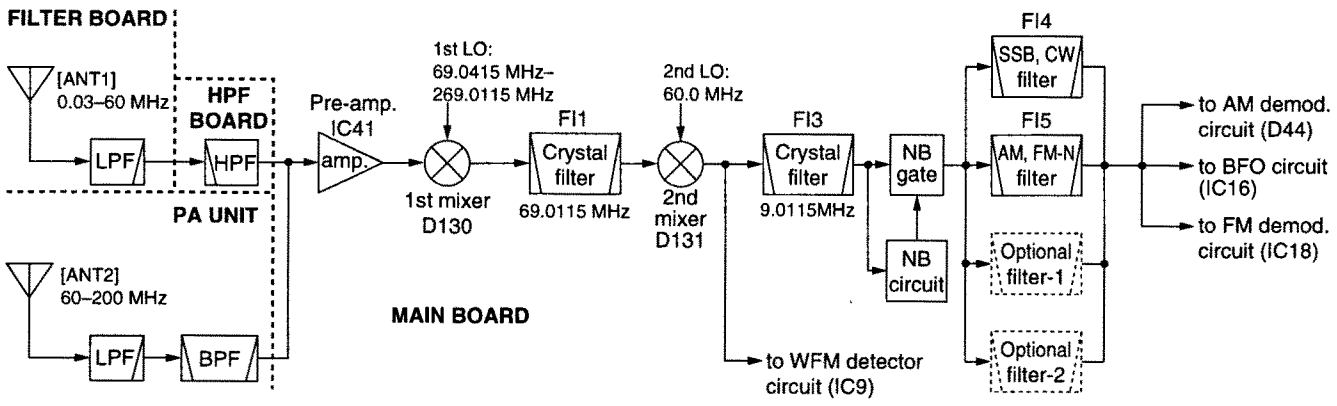
D19, D21, D31 and D33 are varactor diodes that tune the center frequency of an RF passband for wide bandwidth receiving and good image response rejection. When signals above 129 MHz are received, the switching diodes (D20, D22) are turned off by the control signal "LB" from the PLL unit, then the varactor diodes (D33, D31) are disconnected.

3-1-3 PREAMPLIFIER CIRCUIT (MAIN BOARD)

The preamplifier circuit in the IC-706MKII has approx. 15 dB gain over a wideband frequency range.

When the preamplifier is turned ON, the signals from the RF circuit are applied to the preamplifier (IC41) via D122. Amplified or bypassed signals are applied to the 1st mixer circuit (D130).

• RECEIVER CONSTRUCTION



3-1-4 1ST MIXER CIRCUIT (MAIN BOARD)

The 1st mixer circuit mixes the receive signals with the 1st LO signal to convert the receive signal frequencies to a 69 or 70.7 MHz 1st IF.

The signals from the preamplifier circuit, or signals which bypass the preamplifier, are applied to a low-pass filter and then to the 1st mixer (D130).

The 1st LO signals (69.0415–269.0115 MHz) enter the MAIN board from the PLL unit via J4. The LO signal is amplified at Q4, filtered by a low-pass filter, and then, applied to the 1st mixer.

• 1st IF frequency

Mode	Frequency
SSB, FM	69.0115 MHz
CW, RTTY	69.0106 MHz
AM	69.0100 MHz
WFM	70.7000 MHz

3-1-5 1ST IF CIRCUIT (MAIN BOARD)

The 1st IF circuit filters and amplifies the 1st IF signals. The 1st IF signals are applied to a Crystal Filter (FI1) to suppress out-of-band signals.

The 69 MHz 1st IF signals (except WFM) pass through the crystal filter (FI1), however, the 70.7 MHz 1st IF signal (WFM) passes through a bandpass filter (L104–L108, C358–C361). Then the filtered signals are applied to the IF amplifier (IC4).

The AGC voltage is supplied to the transmit/receive switching circuit (D13, D14) and D13/D14 function as PIN attenuators for AGC operation.

The amplified signals are then applied to the 2nd mixer circuit (D131) via the bandpass filter (L109–L112, C364–C367).

3-1-6 2ND MIXER CIRCUIT (MAIN BOARD)

The 2nd mixer circuit mixes the 1st IF signals and 2nd LO signal (60.00 MHz) to convert the 1st IF to a 2nd IF.

The 1st IF signals from the band pass filter (L109–L112, C364–C367) are converted to 9 MHz or 10.7 MHz 2nd IF signals at the 2nd mixer (D131).

The 2nd IF signals are applied to the bandpass filter (FI3) to suppress undesired signals, such as the 2nd LO signal, and are then applied to the noise blanker gate (D20, D21).

• 2st IF frequency

Mode	Frequency
SSB, FM	9.0115 MHz
CW, RTTY	9.0106 MHz
AM	9.0100 MHz
WFM	10.7000 MHz

While in WFM mode, the IF signals pass through the low-pass filter (L52, C82–C84), IF amplifier (Q5), ceramic filter (FI2) and IF amplifier (Q52). The signals are then applied to the WFM demodulator circuit (IC9).

3-1-7 NOISE BLANKER CIRCUIT (MAIN BOARD)

The noise blanker circuit detects pulse type noise, and turns OFF the signal line when noise appears.

A portion of the signals from FI3 are amplified at the noise amplifiers (Q10, Q12, amplifier section of IC9), then detected at the noise detector (D39) to convert the noise components to DC voltages.

The converted voltages are then applied to the noise blanker switch (Q13, Q14). At the moment the detected voltage exceeds Q13's threshold level, Q14 outputs a blanking signal to close the noise blanker gate (D20, D21) by applying reverse-biased voltage.

The detected voltage from D39 is also applied to the noise blanker AGC circuit (Q11, Q16) and is then fed back to the noise amplifier (IC9) as a bias voltage. The noise AGC circuit prevents closure of the noise blanker gate for long periods by non-pulse-type noise. The time constant of the noise blanker AGC circuit is determined by R143 and C459.

The 2nd IF signals from the noise blanker gate are then applied to the 2nd IF circuit.

3-1-8 2ND IF CIRCUIT

The 2nd IF circuit amplifies and filters the 2nd IF signals.

The 2nd IF signals from the noise blanker gate (D20, D21) are amplified at the IF amplifier (IC6) via the Tx/Rx switch (D22) and applied to a 2nd IF filter as shown below.

• Used 2nd IF filter

Mode	Used filter	Control signal
SSB, CW, RTTY AM nar.	FL-272 (FI4)	2F23
AM, FM nar.	FL-94 (FI5)	2F80
FM	Bypassed	2FTH
SSB nar.	Optional FL-223	OP1 or OP2
CW nar., RTTY nar.	Optional FL-100, FL101, FL-223, FL-232	OP1 or OP2
SSB wide, CW wide, RTTY wide	Optional FL-103	OP1 or OP2

The filtered or bypassed signals are applied to the buffer amplifier (Q65), IF amplifiers (Q42, Q43) and buffer amplifier (Q44) to obtain a detectable level at the demodulator circuit

The amplified signals from the buffer amplifier (Q44) are shared between the SSB/CW/RTTY detector (IC16), AM detector (D44) and AGC detector (D43). Output signals from Q65 are applied to the FM IF IC (IC18).

3-1-9 IF SHIFT CIRCUIT (MAIN BOARD)

The IF shift circuit shifts the center frequency of IF signals to electronically shift the center frequency.

The IF shift circuit shifts the 1st LO and BFO within ±1.2 kHz in SSB/CW/RTTY modes or ±250 Hz in CW-N/RTTY-N modes. As a result, the 2nd IF (also 1st IF) is shifted from the center frequency of the 2nd IF filter (FI4, FI5 or optional IF filters). This means 2nd IF signals do not pass through the center of the 2nd IF filter. Therefore, the higher or lower frequency components of the IF are cut out. Since the BFO frequency is also shifted the same value as the 1st IF, frequency is corrected at the detector.

In the IC-706MKII, the 1st LO frequency is shifted to change the 2nd IF because a fixed 2nd LO frequency (60 MHz) is used. The 1st IF filter (FI1) and crystal filter (FI3) have 15 kHz passband widths, and do not affect IF shift operation.

3-1-10 AGC CIRCUIT (MAIN BOARD)

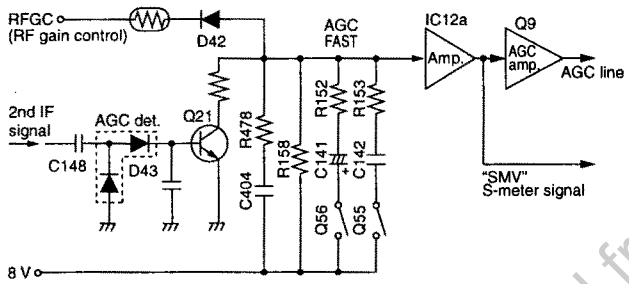
The AGC (Automatic Gain Control) circuit reduces IF amplifier gain to keep the audio output at a constant level. The receiver gain is determined by the voltage on the AGC line (Q9 collector).

The 2nd IF signal from the buffer amplifier (Q44) is detected at the AGC detector (D43) and applied to the AGC amplifiers (Q21, IC12a, Q9). IC12a sets the receiver gain with the [RF/SQL] control via the "RFGC' signal line.

When receiving strong signals, the detected voltage increases and the AGC voltage decreases via the DC amplifier (Q9). The AGC voltage is used for the bias voltage of the transmit/receive switching PIN diodes (D13, D14, D22, D23) to attenuate the received signals.

When AGC slow is selected, C141 and R152 are connected in parallel to obtain appropriate AGC characteristics.

• AGC CIRCUIT



3-1-11 S-METER CIRCUIT (MAIN BOARD)

The S-meter circuit indicates the relative received signal strength while receiving by utilizing the AGC voltage which changes depending on the received signal strength.

The output voltage of the AGC amplifier (IC12a, pin 1) is applied to the main CPU (IC25, pin 30) as an S-meter signal via the "SMV" signal line. The FM S-meter signal from the FM IF IC (IC18, pin 12) is also applied to the main CPU (IC25, pin 30) via Q68.

The S-meter signal from the main CPU (IC25) is applied to the sub CPU and is then displayed on the S-meter readout.

3-1-12 SQUELCH CIRCUIT (MAIN BOARD)

The squelch circuit mutes audio output when the S-meter signal is lower than the [RF/SQL] control setting level.

The S-meter signal is applied to the main CPU (IC25 pin 30) in SSB/CW/RTTY modes and is compared with the threshold level set by the [RF/SQL] control. The [RF/SQL] setting is picked up at the sub CPU (DISPLAY board; IC1, pin 99). The main CPU compares the S-meter signal and [RF/SQL] setting, and controls the AF selector switch (IC15) to cut out AF signals via IC27a.

In FM mode, a portion of the AF signals from the FM IF IC (IC18, pin 9) are applied to the active filter section (pin 8) where noise components above 20 kHz are amplified. The signals are rectified at the noise detector section and then output from pin 14. The noise squelch signal from pin 14 is applied to the main CPU (pin 31) via the "NSQV" signal line. The CPU then controls the AF selector switch (IC15).

3-1-13 DEMODULATOR CIRCUITS (MAIN BOARD)

(1) SSB/CW/RTTY modes

The 2nd IF signals from the buffer amplifier (Q44) are mixed with the BFO signal from the PLL unit at the product detector (IC16, pin 6). The detected AF signals from IC16 (pin 3) are applied to the AF selector switch (IC15, pin 12).

(2) AM mode

The 2nd IF signals from the buffer amplifier (Q44) are detected at the AM detector (D44). The detected AF signal is applied to the AF selector switch (IC15, pin 15).

(3) FM/FM NARROW modes

The 2nd IF signals from the buffer amplifier (Q65) are applied to the FM IF IC (IC18, pin 16) where the IF signals are converted into 455 kHz IF signals. The signals pass through FI6 and are applied to the quadrature detector section. X1 is used for quadrature detector. The detected AF signals from pin 9 are then applied to the AF selector switch (IC15, pin 14) via the de-emphasis circuit (IC12b).

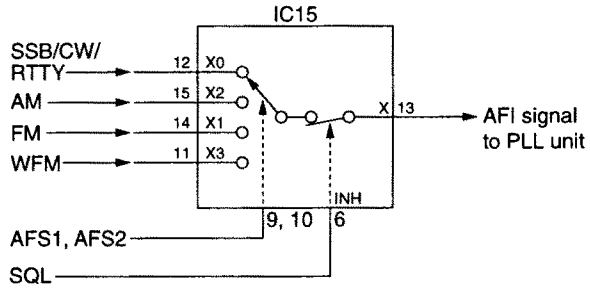
(4) WFM mode

The 2nd IF signals from the IF amplifier (Q5) pass through FI2, are amplified at Q52 and are then applied to the FM IF IC (IC9, pins 2, 3) where the IF signals are converted into AF signals. The detected AF signals from pin 8 are then applied to the AF selector switch (IC15, pin 11).

3-1-14 AF SELECTOR SWITCH (MAIN BOARD)

The AF signals from one of the detector circuits are applied to the AF selector switch (IC15). IC15 consists of dual 4-channel analog switches which are selected with a mode signal and the squelch control signal.

• AF selector switch



3-1-15 AF AMPLIFIER CIRCUIT (PLL UNIT)

The AF amplifier amplifies the demodulated signal to a suitable driving level for the speaker.

The AF signals from the AF selector switch (MAIN board; IC15) are applied to the PLL unit via the "AFI" signal line. The CW side tone/beep tone and optional synthesized voice are also applied to the PLL unit via the "AFBP" signal line.

The AF signals from the MAIN board are applied to the VCA (Voltage Controlled Amplifier) circuit (IC4). The AF gain setting from the main CPU is converted to DC voltage at the D/A converter (MAIN board IC35) and applied to the VCA control terminal (IC4, pin 8) via the "AFGC" signal line. The output AF signal from IC4 (pin 9) is power-amplified at IC5 to drive the speaker.

3-2 TRANSMITTER CIRCUITS

3-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN BOARD)

The microphone amplifier circuit amplifies microphone input signals and outputs the amplified signals to the balanced modulator or FM modulation circuit.

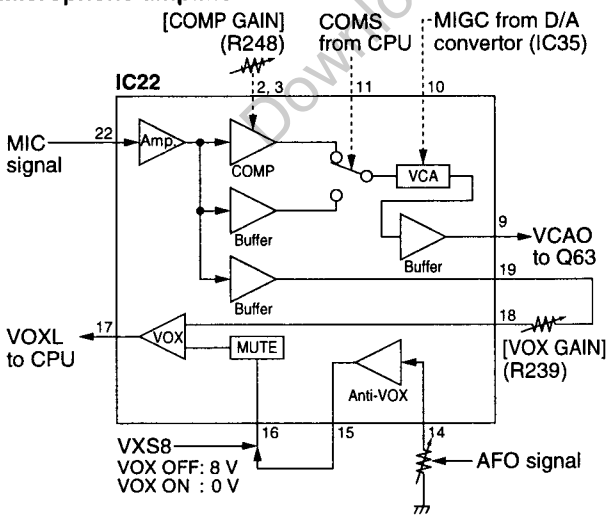
Audio signals from the front or rear panel [MIC] connector enter the microphone amplifier IC (IC22, pin 22) and are then amplified at the microphone amplifier or speech compressor section. Compression level is adjusted with the [COMP GAIN] control (R248).

The amplified or compressed signals are applied to the VCA section of IC22. The microphone gain setting from the D/A converter (IC35, pin 11) is applied to the VCA control terminal (IC22, pin 10). The resulting signals from pin 9 are then applied to the buffer amplifier (Q63). External modulation input from the [ACC] socket (pin 11) is also applied to Q63.

While in SSB mode, the amplified signals from the buffer amplifier (Q63) are applied to the AF selector switch (IC23) and then to the balanced modulator (IC17).

While in AM/FM mode, the amplified signals from the buffer amplifier (Q63) are applied to the limiter amplifier (IC24a) and splatter filter (IC24b). The signals are then applied to the AF selector switch (IC23) in AM mode or to the varactor diode (D67) in FM mode.

• Microphone amplifier



3-2-2 VOX CIRCUIT (MAIN BOARD)

The VOX (Voice-Operated-Transmission) circuit sets transmitting conditions according to voice input. The microphone amplifier IC (IC22) includes the VOX circuit.

The microphone signals from IC22 (pin 19) pass through the [VOX GAIN] control (R239) and are then applied to the VOX comparator section (IC22, pin 18) to switch the keying input of the main CPU (IC25, pin 15). When voice levels exceed the reference level, the VOX circuit sets the transceiver to transmit.

On the other hand, a speaker drive signal from the AF power amplifier (PLL unit IC5) is applied to the anti-VOX comparator section (IC22, pin 14) via the [ANTI VOX] control (R244). When the audio output level increases, this comparator cuts outs the VOX comparator via the MUTE terminal (IC22, pin 16).

3-2-3 BALANCED MODULATOR (MAIN BOARD)

The balanced modulator converts the AF signals from the microphone amplifier to a 9 MHz IF signal with a BFO (Beat Frequency Oscillator) signal.

Microphone signals from the AF selector switch (IC23) are applied to the balanced modulator (IC17 pin 6). The BFO signal from the PLL unit is applied to IC17 (pin 8) as a carrier signal.

IC17 is a double balanced mixer IC and outputs a double side band (DSB) signal with –40 dB of carrier suppression. R191 and R193 adjust the balanced level of IC17 for maximum carrier suppression. The resulting signal passes through a 9 MHz IF filter (FI4 in SSB/CW/RTTY modes) to suppress unwanted sideband signals.

In AM mode, R195 is connected to upset the balance of IC17 via Q23 for leaking the BFO signal as a carrier signal. The CW keying/RTTY TX signal is applied to IC17 pin 6.

3-2-4 FM MODULATION CIRCUIT (MAIN BOARD)

The microphone signals from Q63 are applied to the limiter amplifier (IC24a) and the splatter filter (IC24b). The 1750 Hz European tone signal from the main CPU (IC25 pin 40) is also applied to IC24a pin 2 for European repeaters. The subaudible tone signal (67.0–254.1 Hz) from the main CPU (IC25 pin 37) is also applied to IC24b pin 5 for repeater use.

The resulting signals are applied to the VCO circuit (Q40, D67) via R274 to change the reactance of the varactor diode (D67) for FM modulation. The modulated signal is buffer-amplified at Q41 and bypasses the 9 MHz IF filter.

3-2-5 TRANSMITTER IF CIRCUIT (MAIN BOARD)

The 9 MHz IF signal from the modulation circuit passes through the 9 MHz IF filter (FI4 in SSB/CW/RTTY modes; FI5 in AM/FM-N modes; through in FM mode). The signal is amplified at IC6, and then passes through the total gain adjustment volume (R511), and the crystal filter (FI3). The signal is then applied to the 2nd mixer (D131).

The signal is mixed with the 2nd LO signal (60 MHz) and converted to a 69 MHz IF signal at the 2nd mixer (D131). The 69 MHz IF signal passes through a bandpass filter, the IF amplifier (IC4) and the 69 MHz IF filter (FI1) and is then converted to the displayed frequency at the 1st mixer (D130) with the 1st LO signal. The mixers (D130, D131) and IF amplifiers (IC4, IC6) are used commonly for both receiving and transmitting.

The ALC voltage is supplied to the transmit/receive switching circuit (D13/D14 and D22/D23). D13/D14 and D22/D23 function as PIN attenuators for ALC operation.

3-2-6 RF CIRCUIT (PA UNIT, MAIN AND HPF BOARD)

The RF circuit amplifies the displayed frequency signal to obtain 100 W of RF output power for HF/50 MHz bands and 20 W for the 144 MHz band.

The HF/50 MHz RF signal from the 1st mixer (D130) via the low-pass filter enters the HPF board and then passes through one of 6 high-pass filters (Refer to 3-1 for used RF high-pass filter.). The 50 MHz RF signal passes through a low-pass filter additionally. The filtered signal returns to the MAIN board, is amplified at the YGR amplifier (IC1), and is then applied to the PA unit.

The 144 MHz RF signal from the 1st mixer (D130) via the low-pass filter bypasses the filters in the HPF board via the "TOTR" line and passes through the bandpass filter (L99–L101, C329–C333) in the MAIN board, The signal is amplified at the RF amplifier (IC38) and YGR amplifer (IC1) and is then applied to the PA unit.

The signal from IC1 enters the PA unit and is amplified at the predrive amplifiers (Q16, Q1) and drive amplifier (Q4) in sequence. The amplified signal is applied to the band switch (RL1).

The HF/50 MHz RF signal from the band switch (RL1) is amplified at a power amplifier (Q41, Q42) to obtain a stable 100 W of RF output power. The power amplified signal is then applied to the [ANT1] connector via one of the low-pass filters in the FILTER board.

For the 144 MHz RF signal from the band switch (RL1), 20 W of RF output power is obtained at the power amplifier (Q43) and the signal is applied to the [ANT2] connector via the antenna switching circuit and low-pass filter.

3-2-8 ALC CIRCUIT (MAIN BOARD)

The ALC (Automatic Level Control) circuit reduces the gain of IF amplifiers in order for the transceiver to output a constant RF power set by the RF power setting even when the supplied voltage shifts, etc.

The HF/50 MHz RF power signal level is detected at the power detector (FILTER board; D9), buffer-amplified at IC1b and applied to the MAIN board as the "FOR" voltage. The 144 MHz RF power signal level is detected at the power detectors (PA unit; D2, D3) and applied to the MAIN board as the "VFOR" voltage.

The "FOR" and "VFOR" voltages are combined to the "FORV" voltage and then applied to IC7b (pin 6). The "POC" voltage from the D/A converter (IC35, pin 12), determined by the RF power setting, is applied to IC7b (pin 5) as the reference voltage.

When the "FORV" voltage exceeds the "POC" voltage, ALC bias voltage from IC7a (pin 1) controls the PIN diodes (D13, D14, D22, D23) using Q39. This adjusts the output power to the level determined by the RF power setting until the "FORV" and "POC" voltages are equalized.

In AM mode, IC7a operates as an averaging ALC amplifier with Q69 and C116. Q64 turns ON and the "POC" voltage is shifted for 40 W AM output power (maximum, 8 W for 144 MHz band) through R499.

The ALC bias voltage from IC7a is also applied to the main CPU (IC25 pin 34) as "ALCV" voltage for ALC meter indication.

An external ALC input (minus voltage) from the [ACC] socket (pin 6) is shifted to plus voltage at D70 and is applied to the buffer amplifier (Q8). External ALC operation is identical to that of the internal ALC.

3-2-9 APC CIRCUIT (MAIN BOARD)

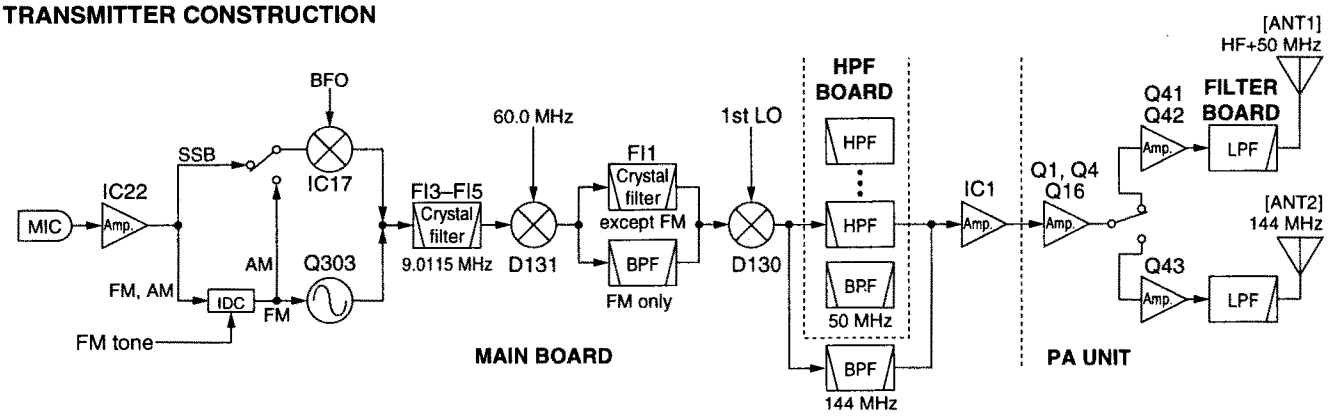
The APC (Automatic Power Control) circuit protects the power amplifiers on the PA unit from high SWR and excessive current for the HF/50 MHz bands.

The reflected wave signal appears and increases on the antenna connector when the antenna is mismatched. The HF/50 MHz reflected signal level is detected at D10 (FILTER board), buffer-amplified at IC1a and applied to the MAIN board as the "REFV" voltage.

When the "REFV" signal level increases, IC7c decreases the ALC voltage via IC7a to activate the ALC.

For the current APC, the driving current at the power amplifier is detected in the voltages ("ICH" and "ICL") which appear at both terminals of a 0.012 Ω resistor (R35) on the PA unit. The detected voltages are applied to the differential amplifier (IC7d pins 12, 13). When the current of the power amplifier exceeds 22 A, IC7d controls the ALC line via IC7a to prevent excessive current flow.

• TRANSMITTER CONSTRUCTION



3-2-10 RF, ALC, SWR METER CIRCUITS (MAIN BOARD)

While transmitting, RF, ALC or SWR meter readings are available and can be selected with the [MET] switch.

(1) Power meter

The "FOR" and "VSOR" voltages are combined to "FORV" voltage and it is then applied to the main CPU (IC25 pin 32) for indicating the output power.

(2) ALC meter

The ALC bias voltage from IC7a pin 1 is applied to the main CPU (IC25 pin 34) for indicating the ALC level.

(3) SWR meter

The "FORV" and "REFV" voltages are applied to the main CPU pins 32 and 33, respectively. The main CPU compares the ratio of "FORV" to "REFV" voltage and indicates the SWR for the [ANT1] connector.

3-3 PLL CIRCUITS

3-3-1 GENERAL

The PLL unit generates a 1st LO frequency (69.0415–269.0115 MHz), a 2nd LO frequency (60 MHz), a BFO frequency (9.01 MHz), an FM 3rd LO frequency (9.4665/9.4650 MHz) and a TX FM PLL reference frequency (9.0115/9.0100 MHz).

The 1st LO PLL adopts a mixerless dual loop PLL system and has 2 VCO circuits. The BFO uses a DDS and the 2nd LO uses a fixed frequency double that of the crystal oscillator.

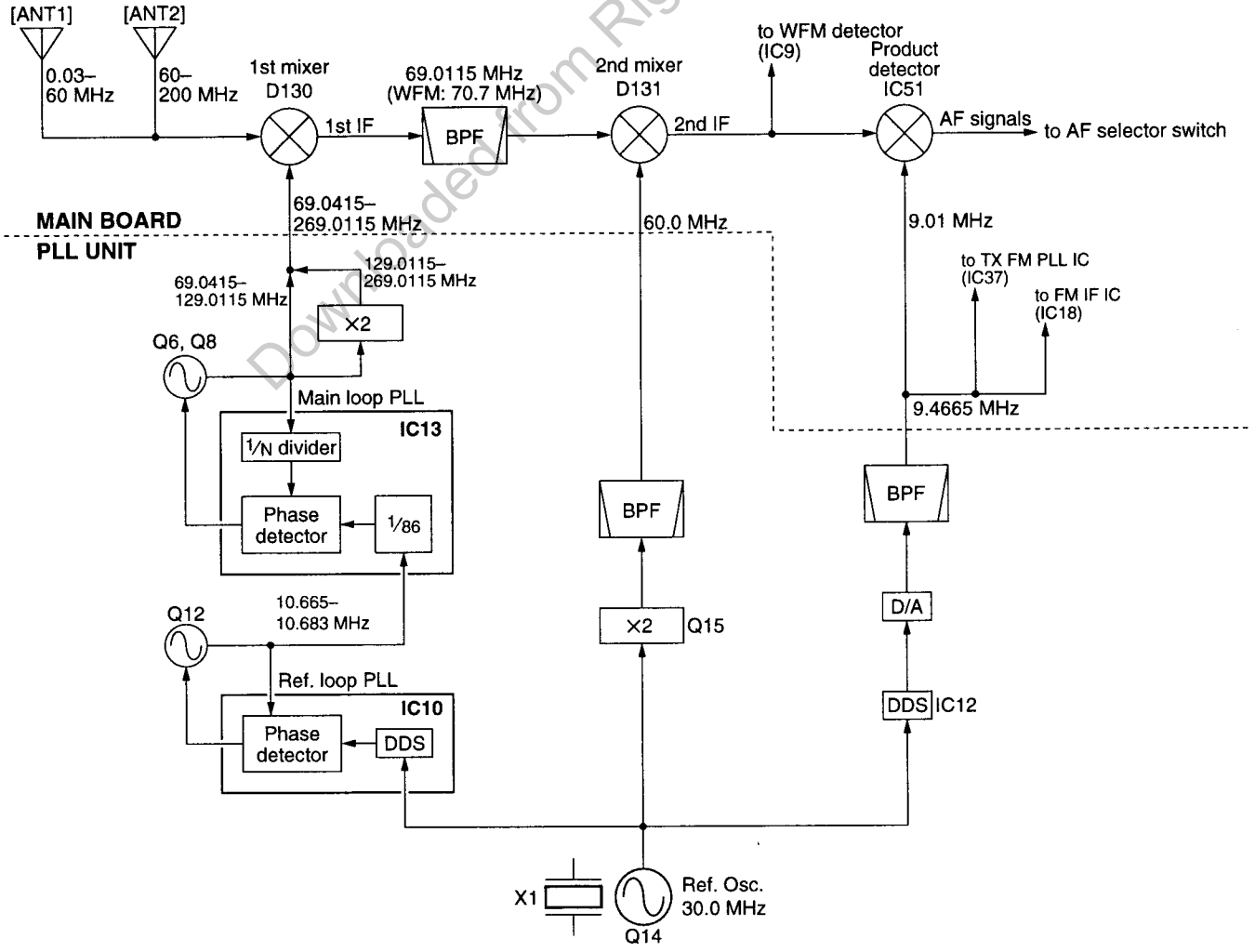
3-3-2 1ST LO PLL CIRCUIT

The 1st LO PLL contains a main loop and reference loop forming a dual loop system.

The reference loop generates a 10.6605 to 10.683 MHz frequency using a DDS circuit, and the main loop generates a 69.0415 to 134.50575 MHz frequency using the reference loop frequency.

While operating on 60 MHz and above, the output is doubled at D8 for oscillating a wide frequency range.

• FREQUENCY CONSTRUCTION



(1) REFERENCE LOOP PLL

The oscillated signal at the reference VCO (Q12, D13) is amplified at the amplifiers (Q13, Q16) and is then applied to the DDS IC (IC 10, pin 46). The signal is then divided and detected on phase with the DDS generated frequency.

The detected signal output from IC10 (pin 56) is converted into a DC voltage (lock voltage) at the loop filter (R88, R203, C132) and then fed back to the varactor diode (D13) in the VCO circuit.

(2) MAIN LOOP PLL

The oscillated signal at one of the main loop VCOs (Q6, Q8) is amplified at the buffer amplifiers (Q10, Q36) and is then applied to the PLL IC (IC13 pin 8). The signal is then divided and detected on phase with the reference loop output frequency.

The detected signal output from IC13 (pin 12) is converted into a DC voltage (lock voltage) at the active loop filter (Q47–Q49) and then fed back to one of the varactor diodes (D4, D6) in the VCO circuits. While operating on 60 MHz and above, the VCO output is doubled at D8 and amplified at Q37.

The oscillated signal passes through a low-pass or bandpass filter and is then applied to the MAIN board as a 1st LO signal.

3-3-3 2ND LO AND REFERENCE OSCILLATOR CIRCUITS

The reference oscillator (X1, Q14) generates a 30.0 MHz frequency used for the 1st LO and BFO circuits as a system clock and for the 2nd LO signal.

The oscillated signal is buffer-amplified at Q27, doubles at Q15 and the 60 MHz frequency is picked up at the bandpass filter (L37, L38). The 60 MHz signal is applied to the MAIN board as a 2nd LO signal.

3-3-4 BFO CIRCUIT

The DDS IC (IC12) generates a 10-bit digital signal. The signal is converted to an analog wave signal at the D/A converter (R116–R135). The analog wave is passed through the high-pass filter and low-pass filter. The 9 MHz BFO signal is then applied to the MAIN board via the "BFO" signal line.

While transmitting in RTTY mode, the RTTY keying signal is applied to IC12 pin 3 to shift the generated frequency and to obtain 2 frequencies for FSK operation.

While receiving in FM or FM narrow mode, the BFO circuit generates a 9.4665 MHz frequency as the 3rd LO signal.

While transmitting in FM or FM narrow mode, the BFO circuit generates a 9.0115 MHz or 9.0100 MHz frequency as the TX FM PLL reference frequency, respectively.

• BFO frequency

Mode	RX BFO/3rd LO frequency [MHz]	TX BFO/FM PLL ref. frequency [MHz]
USB	9.0130	9.0130
LSB	9.0100	9.0100
CW	9.0106 (–CW pitch frequency)	9.0106 (–CW pitch frequency)
CW-R	9.0106 (+CW pitch frequency)	9.0106 (+CW pitch frequency)
RTTY	9.008375 (2125 Hz tone) 9.008885 (1615 Hz tone)	9.0105 (MARK)
AM	No output	9.0100
FM	9.4665 (3rd LO)	9.0115 (PLL ref.)
FM nar.	9.4650 (3rd LO)	9.0100 (PLL ref.)
WFM	No output	No output

IF shift: Center RTTY: Normal polarity

3-4 LOGIC CIRCUITS

3-4-1 BAND SELECTION DATA (MAIN BOARD AND PLL UNIT)

To select the correct RF low-pass filter, high-pass filter and VCOs on the PLL unit, the CPU outputs the following band selection data from the I/O expander (MAIN board; IC35) or DDS IC (PLL unit; IC10) depending on the displayed frequency.

The A/D converter output from IC35 pin 5 is doubled at IC34a to obtain the band voltage for external equipment.

• Band selection data

Frequency [MHz]	IC31, IC32 (MAIN)		IC35 (MAIN)	IC10 (PLL)	
	HPF BPF	LPF	1/2 band voltage	VCO	LPF BPF
0.03–1.999999	L1	L1	3.76 V	VCO0	LOF1
2.0–3.999999	L2	L2	3.08 V		
4.0–7.999999	L3	L3	2.57 V		
8.0–10.999999	L4	L4	0 V		
11.0–14.999999			2.06 V		
15.0–21.999999	L5	L5	1.61 V		
22.0–29.999999	L6	L6	1.12 V		
30.0–39.999999	B7W	L7	0.61 V	VCO1	LOF2
40.0–59.999999	B7				
60.0–128.999999	B8W	L8		VCO0	LOF3
129.0–143.9999				VCO1	LOF4
144.0–148.0000	B8				LOF5
148.000001–200.000000	B8W				LOF4

3-4-2 MAIN CPU PORT ALLOCATIONS (MAIN board IC25)

Pin number	Port name	Description
13	DSHL	Input port for the external paddle (DASH). Low : During key down
14	DOTL	Input port for the external paddle (DOT) or straight key. Low : During key down
15	SNDL	Input port for the [RTTY] or [MIC] connector. High : While transmitting.
16	KEY	Input port for transmit control signal from the optional AT-180/AH-3 antenna tuners.
17	STRT	Input port for the optional AH-3 antenna tuner connection detection. High : When AH-3 is connected.
18	SQLS	Outputs a squelch control signal for the external unit.
19	PWK	Input port for the [POWER] switch. Low : When the [POWER] switch is pushed.
20	POWS	Outputs a power ON signal for the optional AH-3 antenna tuner. High : While power is ON.
21	ATST	Outputs start signal for the optional AT-180 anttena tuner.
22	BEEP	Output port : Beep audio signals while receiving. : CW side tone signals while transmitting.
23	AHST	Outputs start signal for the optional AH-3
24	AFMS	Outputs squelch mute control signal, applied to the AF selector switch (MAIN board; IC15). High : During squelch open.
30	SMV	S-meter level input port for squelch control.
31	NSQV	Noise level input port for squelch control in FM mode.
32	FORV	Forward RF power level input port for SWR meter indications.
33	REFV	Reflected RF power level input port for P0 and SWR meter indication.
34	ALCV	ALC level input port for ALC meter indication.
37	TONE	Outputs subaudible tone signals.
39	BUSY	Input port for the optional UT-102 (Voice synthesizer unit) activation signal. High : During speech synthesis.
40	ETON	Outputs 1750 Hz European tone signal.

MAIN CPU PORT ALLOCATIONS (continued)

Pin number	Port name	Description
41	SPST	Outputs a strobe signal for the optional UT-102 (Voice synthesizer unit).
42	IDT	Outputs serial data for the I/O expanders, optional AT-180/UT-102.
43	ICK	Outputs a clock signal for the I/O expanders, optional AT-180/ UT-102.
44	IBST	Outputs a strobe signal for the I/O expander ICs (IC31, IC32).
45	IMST	Outputs a strobe signal for the I/O expander IC (IC30).
46	IAST	Outputs a strobe signal for the D/A converter IC (IC35).
48	PBST	Outputs a strobe signal for the BFO DDS IC (PLL unit; IC12).
49–51	CON2–CON0	Output mode control signals for the 1st LO DDS IC (PLL unit; IC10).
52	PDST	Outputs a strobe signal for the 1st LO DDS IC (PLL unit; IC10).
53	PCE	Outputs a strobe signal for the 1st LO PLL IC (PLL unit; IC13).
54	PDT	Outputs serial data for the DDS ICs (PLL unit; IC10, IC12) and PLL IC (PLL unit; IC13).
55	PCK	Outputs a clock signal for the DDS ICs (PLL unit; IC10, IC12) and PLL IC (PLL unit; IC13).
65	MCK	Input port for microphone ON/OFF switch.
66	MUD	Input port for microphone up/down switches.
74	SNDS	Input port for transmit/receive switching signals for the [ACC] connector. Low : While transmitting.
75	KDS	Outputs a CW keying signal or RTTY TX signal.
78	CTXD	Output port for CI-V bus line.
79	CRXD	Input port for CI-V bus line.

3-4-3 SUB CPU PORT ALLOCATIONS

(DISPLAY board IC1)

Pin number	Port name	Description
1	SFTV	Input port for the [SHIFT] control.
18	PTTS	Outputs a PTT signal. Low : While transmitting.
19	AMBS	Outputs ON/OFF control signal for the display backlight. High : While display backlight is turned ON.
20	DIMS	Outputs a brightness control signal for the display backlight. High :While display backlight is dark.
80	PHNL	Input port for the [PHONES] jack connection detection. High : When the headphone or external speaker is connected to the [PHONES] jack.
81	RITK	Input port for the [RIT] switch.
96	PTTV	Input port for the [PTT] switch on the microphone.
97	MUDV	Input port for the microphone up/down signal.
98	AFGV	Input port for the [AF] control.
99	SQLV	Input port for the [RF/SQL] control.
100	RIT	Input port for the [RIT] control.

3-4-4 I/O EXPANDER PORT ALLOCATIONS

MAIN board IC30

Pin number	Port name	Description
4	MODS	Outputs select signal for the Tx AF selector switch (IC23). Hign : When AM and SSB modes are selected.
5	AMS	Outputs AM mode select signal. High : When AM mode is selected.
6	FMS	Outputs FM and FM-N modes select signal. High : When FM and FM-N modes are selected.
7	WFMS	Outputs WFM mode select signal. High : When WFM mode is selected.
11, 12	AFS1, AFS2	Output select signals for the Rx AF selector switch (IC15).

PORT	MODE			
	WFM	FM	AM	SSB/CW/RTTY
AFS1	High	High	Low	Low
AFS2	High	High	Low	Low

MAIN board IC30 (continued)

Pin number	Port name	Description
13	UNFM	Outputs non-FM mode select signal. High : When SSB/CW/RTTY/AM modes are selected.
14	MINH	Outputs an audio mute signal for the Tx AF selector switch (IC23). High : While transmitting in CW/RTTY modes.

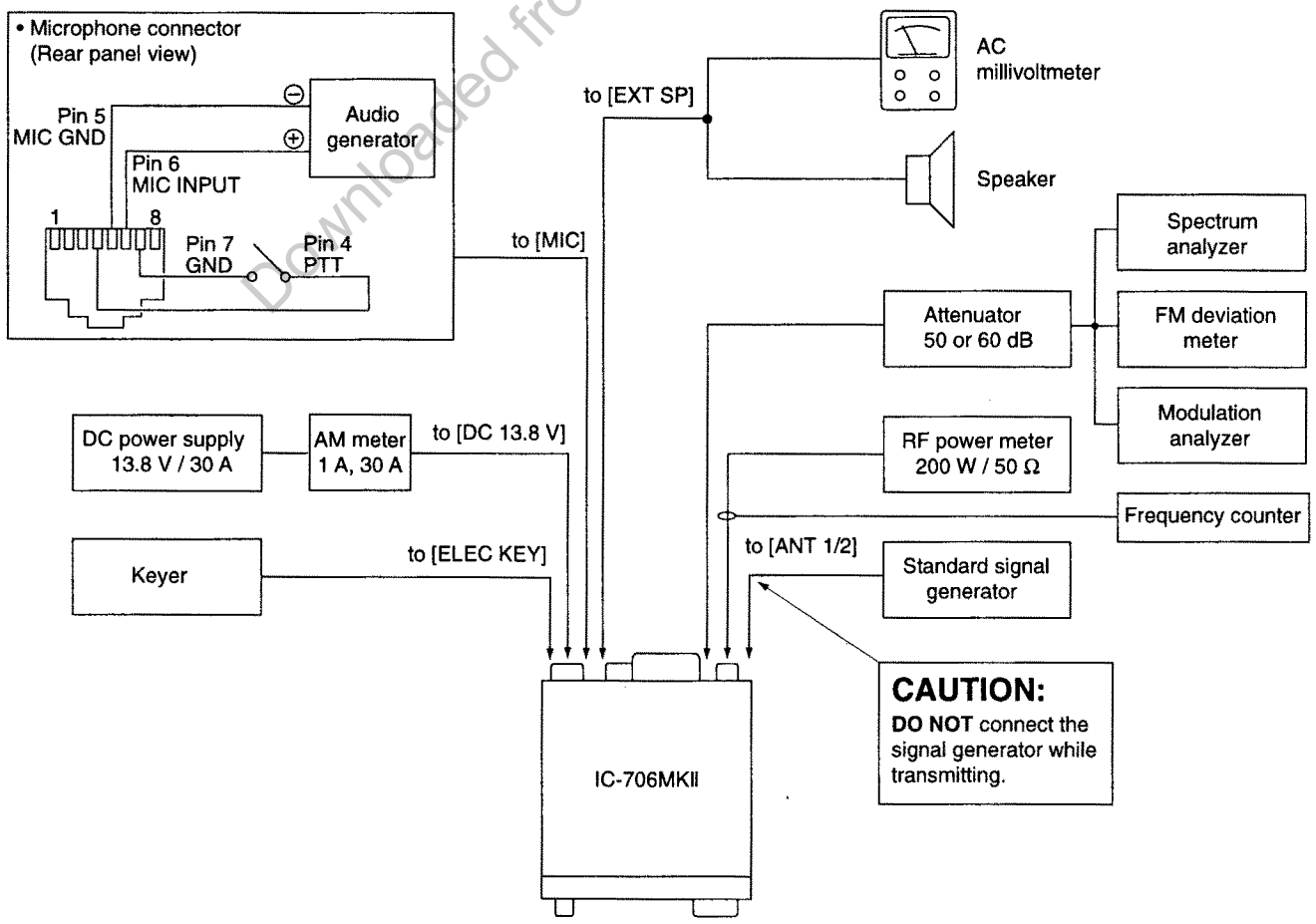
SECTION 4 ADJUSTMENT PROCEDURES

4-1 PREPARATION BEFORE SERVICING

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 13.8 V DC Current capacity : 30 A or more	AC millivoltmeter	Measuring range : 10 mV–10 V
RF power meter (terminated type)	Measuring range : 10–200 W Frequency range : 1.8–200 MHz Impedance : 50 Ω SWR : Less than 1.2:1	DC voltmeter	Input impeadance : 50 kΩ/DC or better
		AM meter	Measurement capabillity: 1 A and 30 A
Frequency counter	Frequency range : 0.1–200 MHz Frequency accuracy: ±1 ppm or better Sensitivity : 100 mV or better	Audio generator	Frequency range : 300–3000 Hz Output level : 1–500 mV
RF voltmeter	Frequency range : 0.1–200 MHz Measuring range : 0.01–10 V	Attenuator	Power attenuation : 50 or 60 dB Capacity : 150 W or more
Digital multimeter	Input impeadance : 10 MΩ/DC or better	Spectrum analyzer	Frequency range : At least 400 MHz Spectrum bandwidth: ±100MHz or more
Standard ignal generator (SSG)	Frequency range : 0.1–200 MHz Output level : 0.1 µV–32 mV (–127 to –17 dBm)	FM deviation meter	Frequency range : At least 200 MHz Measuring range : 0 to ±10 kHz
		Modulation analyzer	Frequency range : At least 150 MHz Measuring range : 0–100 %
Distortion meter	Frequency range : 1 kHz ±10 % Measuring range : 1–100 %	External speaker	Impeadance : 8 Ω Max. Input power : 5 W
Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–10 V		

■ CONNECTION



4-2 PLL ADJUSTMENT

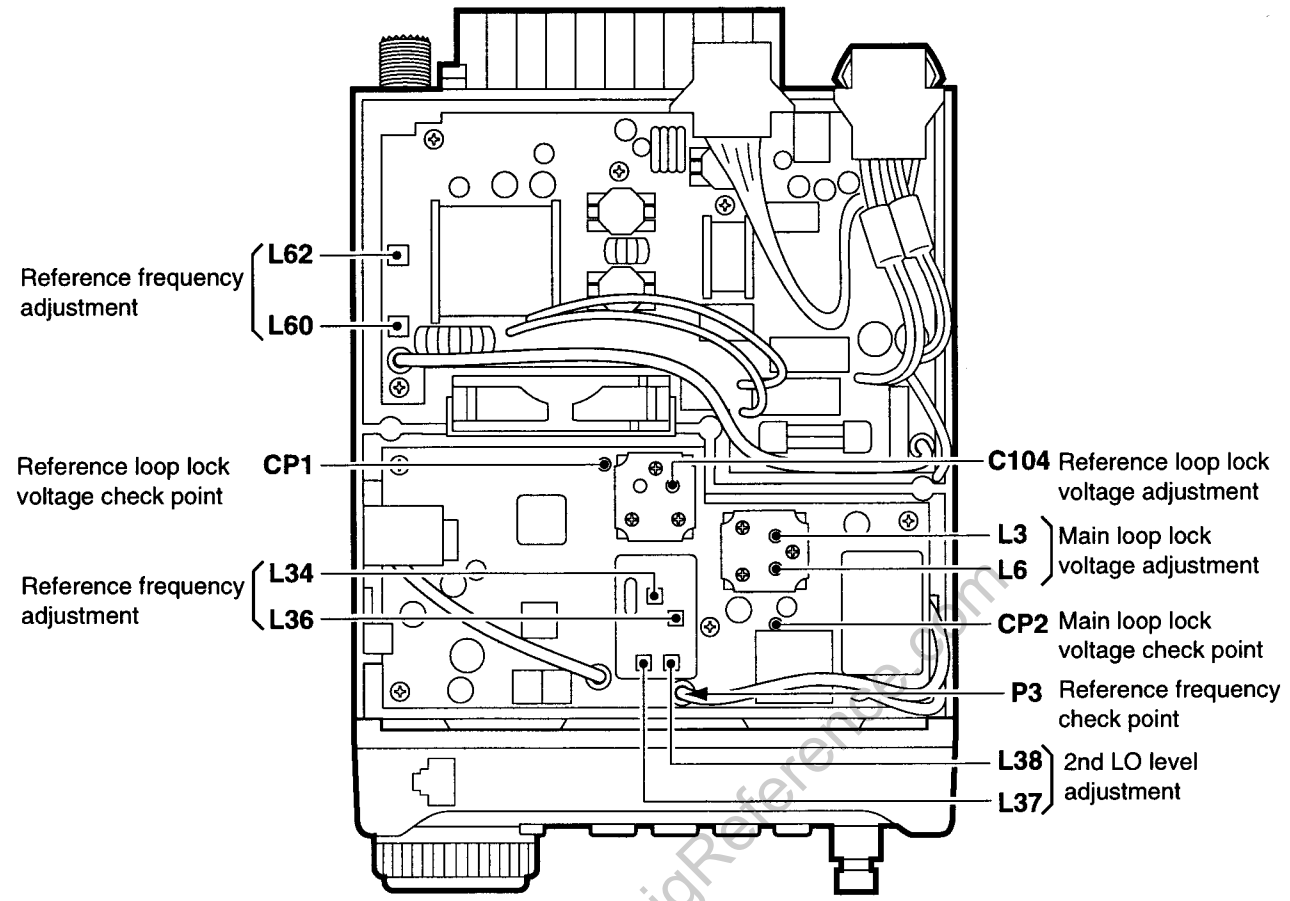
ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
REFERENCE FREQUENCY	1	• Displayed freq. : Any • L36 (PLL unit) : Center • Receiveing	PLL	Connect an RF voltmeter to check point P3.	Maximum level (0 dBm or more)	PLL	L37, L38
	2			Connect a frequency counter to check point P3.	60.000000 MHz		L34, L36
REFERENCE LOOP LOCK VOLTAGE	1	• Displayed freq. : 0.03000 MHz • Mode : USB • Receiving	PLL	Connect a digital multimeter or oscilloscope to check point CP1.	2.0 V	PLL	C104
MAIN LOOP LOCK VOLTAGE	1	• Displayed freq. : 30.00000 MHz • Mode : USB • Receiving	PLL	Connect a digital multimeter or oscilloscope to check point CP2.	1.1 V	PLL	L3
	2	• Displayed freq. : 60.00000 MHz • Receiving			1.1 V		L6

4-3 RECEIVER ADJUSTMENT

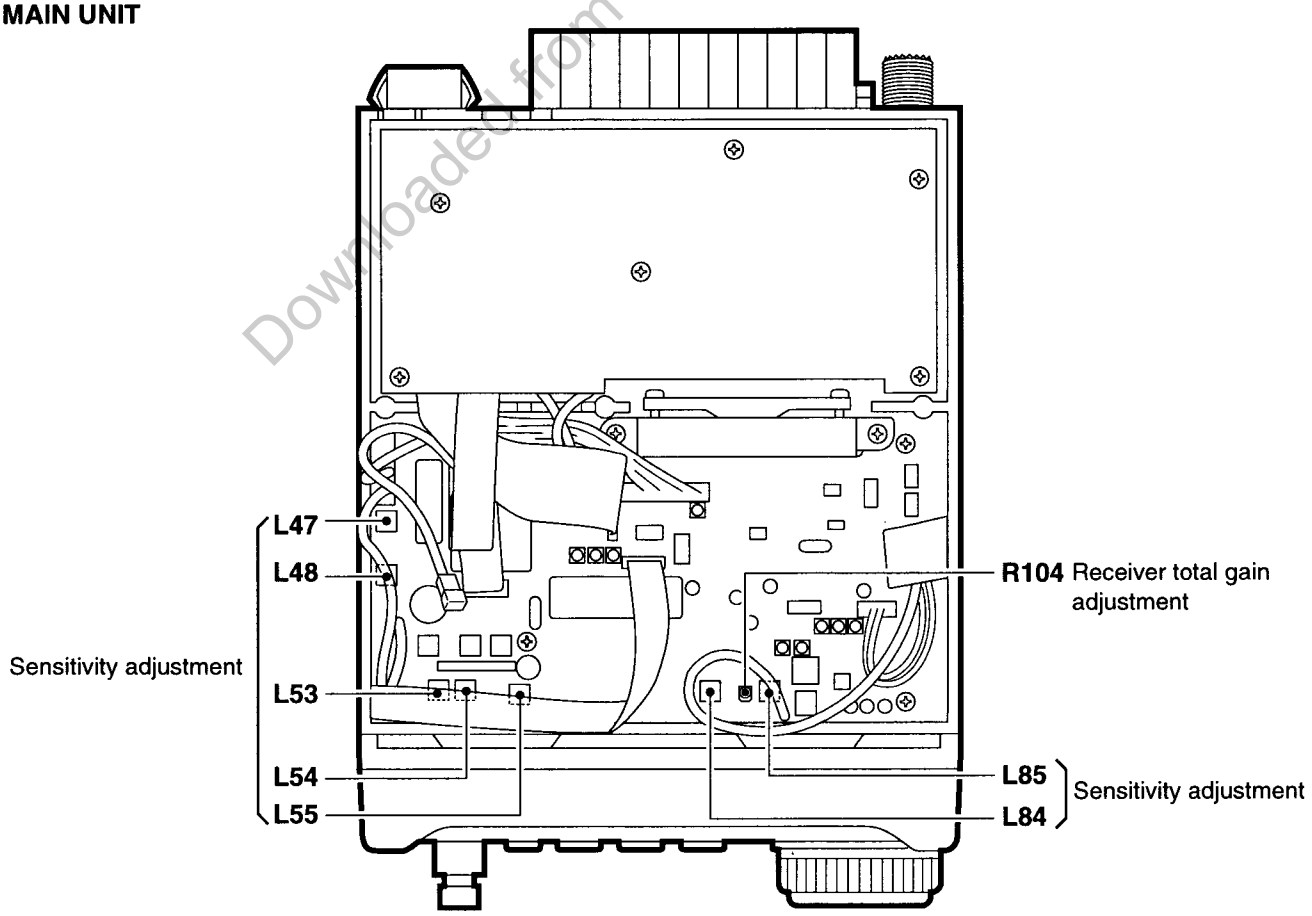
ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
SENSITIVITY	1	• Displayed freq. : 14.10000 MHz • Mode : USB • [RIT] : OFF • [M4 AGC] : Fast (F AGC) • [M3 NB] : OFF • [P.AMP/ATT] : Preamp ON • [VOX GAIN] : Center • [ANTI VOX] : Max counterclockwise • [COMP GAIN] : Center • [BEEP/SIDE T] : Center • Connect a standard signal generator to [ANT 1] and set as: Frequency : 14.10150 MHz Level : 0.5 µV* (–113 dBm) Modulation : OFF • Receiving	Rear panel	Connect an AC millivoltmeter to [EXT SP] jack with an 8 Ω dummy load.	Maximum AF output level	MAIN	Adjust repeatedly L47, L48, L55, L84, L85
	2				0.5 dB decrease from step 1.		L53
	3				0.5 dB decrease from step 2.		L54
	4	• Displayed freq. : 146.00000 MHz • Connect a standard signal generator to [ANT 2] and set as: Frequency : 146.001500 MHz • Receiving			Maximum AF output level	PA	L60, L62
RECEIVER TOTAL GAIN	1	• Displayed freq. : 14.1000 MHz • Mode : USB • [P.AMP/ATT] : Preamp OFF • Connect a standard signal generator to [ANT 1] and set as: Frequency : 14.1015 MHz Level : 0.5 mV* (–53 dBm) and OFF Modulation : OFF • Receiving	Rear panel	Connect an AC millivoltmeter to [EXT SP] jack with an 8 Ω dummy load.	30 dB of AF level difference	MAIN	R401

*This output level of a srandard signal generator (SSG) is indicated as SSG's open circuit.

• PLL AND PA UNITS

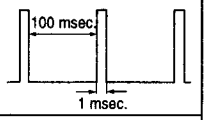


• MAIN UNIT



RECEIVER ADJUSTMENT (CONTINUED)

ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
WFM RECEIVING	1	• Displayed freq. : 80.00000 MHz • Mode : WFM • Connect a standard signal generator to [ANT 2] and set as: Frequency : 80.00000 MHz Level : 0.5 mV* (–53 dBm) • Receiving	MAIN	Connect a digital multimeter or oscilloscope to check point CP1.	4.0 V	MAIN	L63
NOISE BLANKER	1	• Displayed freq. : 14.10000 MHz • Mode : USB • [M3 NB] : OFF • [P.AMP/ATT] : Preamp • R126 (MAIN unit): Center • Connect a standard signal generator to [ANT 1] and set as: Frequency : 14.1015 MHz Level : 1.8 µV* (–82 dBm) and apply noise signal at right to [ANT 1] connector. • Receiving	MAIN	Connect an oscilloscope to check point CP2.	Maximum voltage	MAIN	L61, L64
	2	• [M3 NB] : ON • Receiving			Noise just reduces		R126

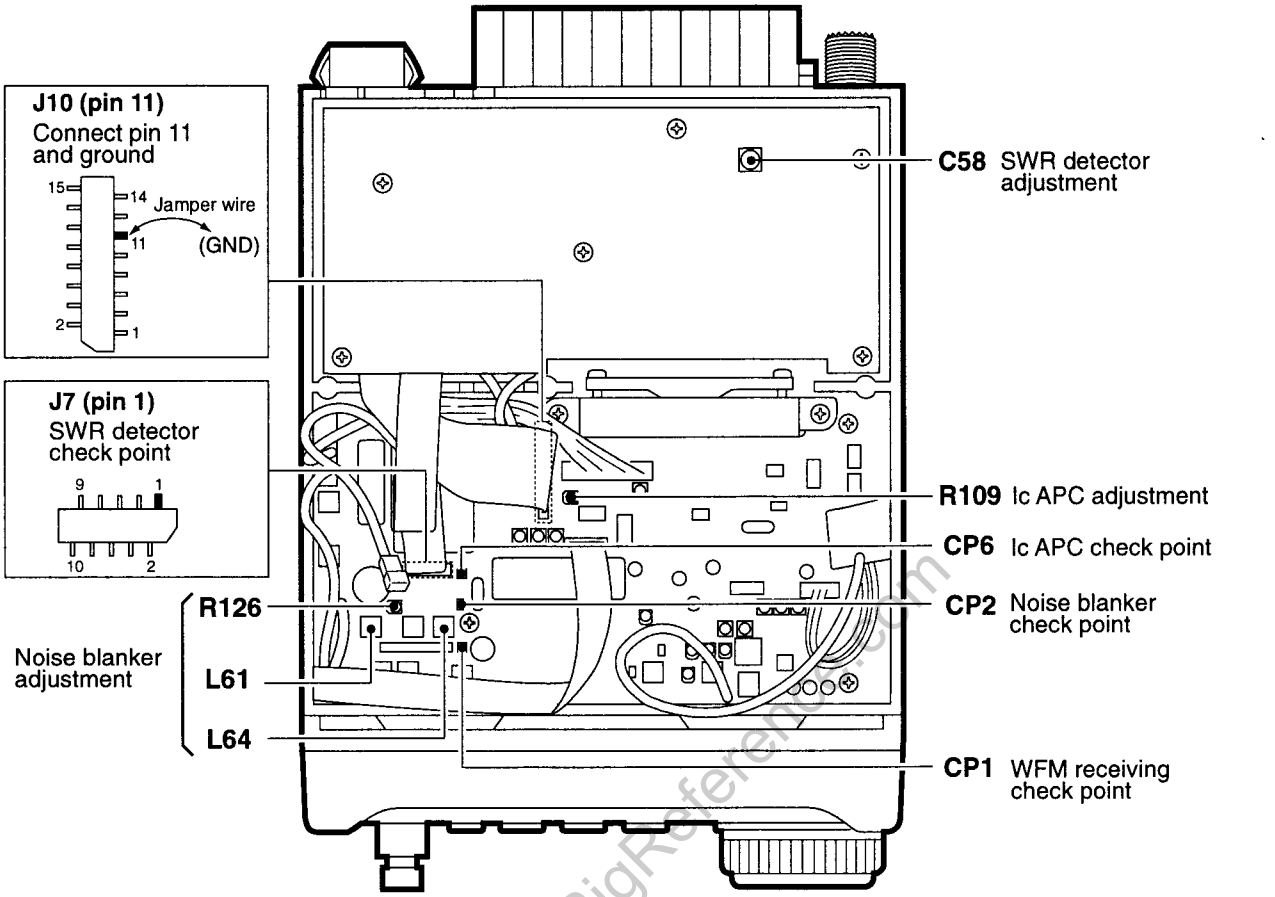


*This output level of a srandard signal generator (SSG) is indicated as SSG's open circuit.

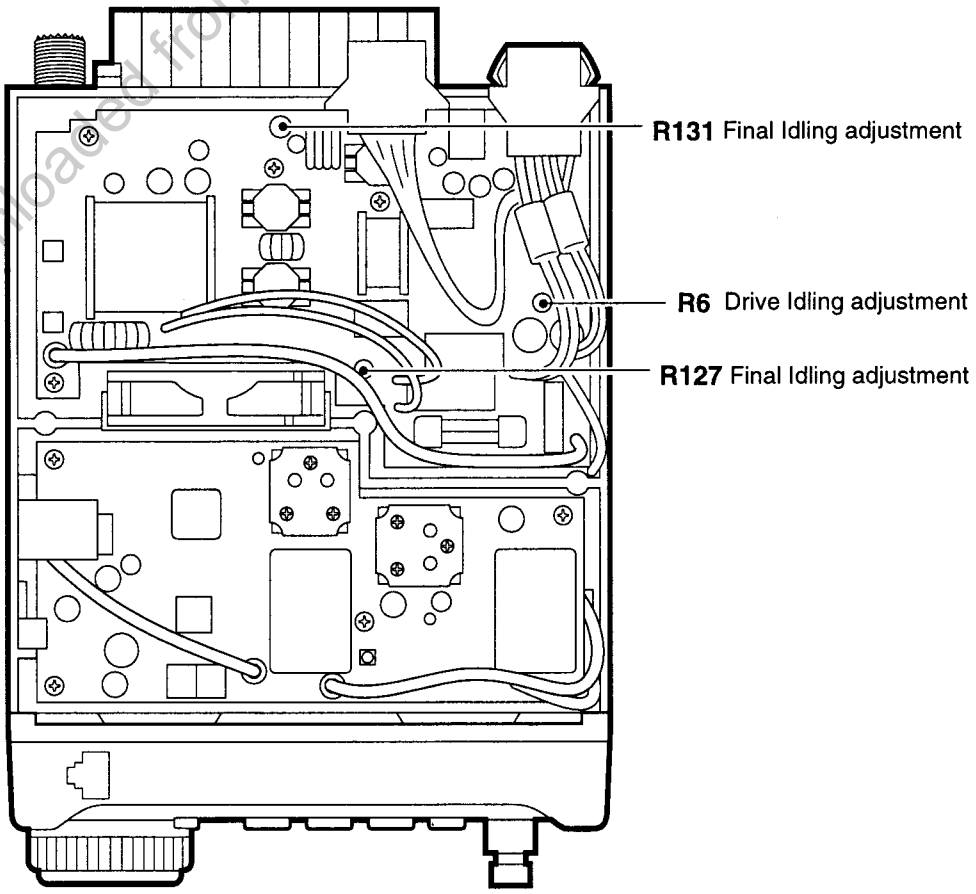
4-4 TRANSMITTER ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
IDLING CURRENT (for drive amplifiers)	1	• Displayed freq. : 14.10000 MHz • Mode : USB • [Q2 MIC GAIN] : 1 (minimum) • R6 (PA unit) : Max. counterclockwise • R131 (PA unit) : Max. counterclockwise • R127 (PA unit) : Max. counterclockwise • Transmitting	PA	Connect a DC ammeter between the DC power supply and transceiver's DC power socket.	1.2 A increase from that R6 is in max. counterclockwise	PA	R6
(for final amplifiers)	2				0.5 A increase from step 1		R131
	3	• Displayed freq. : 145.10000 MHz • Transmitting			1.0 A increase from that R127 is in max. counterclockwise		R127
SWR DETECTOR	1	• Displayed freq. : 14.1000 MHz • Mode : USB • Ground pin 11 of J10 (MAIN unit).	Rear panel	Connect an RF power meter to [ANT 1] connector.	100 W	Quick set mode	Q2 MIC GAIN
	2	• Connect an audio generator to [MIC] connector and set as: 10 mV / 1.5 kHz • Transmitting	MAIN	Connect a digital multimeter to pin 1 of J7.	Minimum voltage	FILTER	C58
	After adjustment, remove the jumper wire from J10.						
Ic APC	1	• Displayed frequency: 3.50000 MHz • Mode : RTTY • [Q1 RF POWER]: H • R95 (MAIN unit) : 3 o'clock position • R109 (MAIN unit): 3 o'clock position • R198 (MAIN unit): Max. clockwise • Ground CP6 with a jumper wire. • Transmitting	Rear panel	Connect a DC ammeter between the DC power supply and transceiver's DC power socket.	22 A	MAIN	R109
	After adjustment, remove the jumper wire from CP6.						

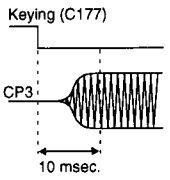
• MAIN AND FILTER UNITS



• PA UNIT



TRANSMITTER ADJUSTMENT (CONTINUED)

ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
TRANSMIT TOTAL GAIN	1	• Displayed freq. : 14.10000 MHz • Mode : USB • [Q1 RF POWER] : H • [Q2 MIC GAIN] : 5 • Connect an audio generator to [MIC] connector and set as: 10 mV / 1.5 kHz • Transmitting	Rear panel	Connect an RF power meter to [ANT 1] connector.	50 W	MAIN	R511
CARRIER SUPPRESSION	1	• Displayed freq. : 14.10000 MHz • Mode : USB and LSB • Apply no AF signal to [MIC] connector. • Transmitting	Rear panel	Connect a spectrum analyzer to [ANT 1] via an attenuator.	Minimum carrrier level	MAIN	Adjust repeatedly R191, R193
OUTPUT POWER	1	• Displayed freq. : 14.10000 MHz • Mode : USB • [Q2 MIC GAIN] : 5 • Connect an audio generator to [MIC] connector and set as: 100 mV / 1.5 kHz • Transmitting	Rear panel	Connect an RF power meter to [ANT 1] connector.	100 W	MAIN	R95
	2	• Displayed freq. : 52.00000 MHz • Transmitting			100 W		R98
	3	• Displayed freq. : 145.00000 MHz • Transmitting		Connect an RF power meter to [ANT 2] connector.	20 W		R338
CW CARRIER LEVEL	1	• Displayed freq. : 14.10000 MHz • Mode : CW • [Q1 RF POWER] : H • [Q5 KEY SPEED] : 60 • [M4 BRK] : BK (semi break-in) • CW paddle : n • Transmit dots for a while using a paddle.	MAIN	Connect an osilloscope to check point CP3 and C177.	Adjust as follows:  	MAIN	R198
FM VCO	1	• Displayed freq. : 29.10000 MHz • Mode : FM • [M4 TON] : OFF • [Q1 RF POWER] : H • Apply no signal to [MIC] connector. • Transmitting	MAIN	Connect a digital multimeter to check point CP4.	1.8 V	MAIN	C267
FM DEVIATION	1	• Displayed freq. : 29.10000 MHz • Mode : FM • [M4 TON] : OFF • [Q1 RF POWER] : H • [Q2 MIC GAIN] : 5 • R260 (MAIN unit) : Center • Connect an audio generator to [MIC] connector and set as: 300 mV / 1 kHz • Transmitting	Rear panel	Connect an FM deviation meter to [ANT 1] via an attenuator.	±4.5 kHz	MAIN	R274
	2	• Set the audio generator as: 10 mV / 1 kHz • Transmitting			±3.5 kHz		R260