REVISED EDITION

TRIO

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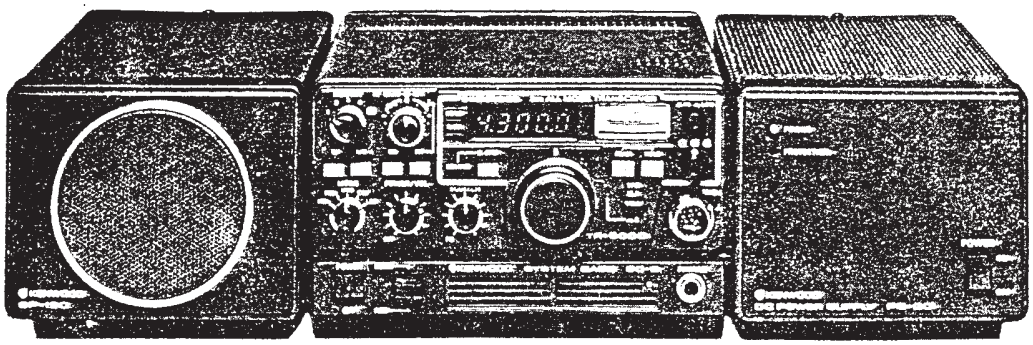
SERVICE MANUAL

Model TR-9000

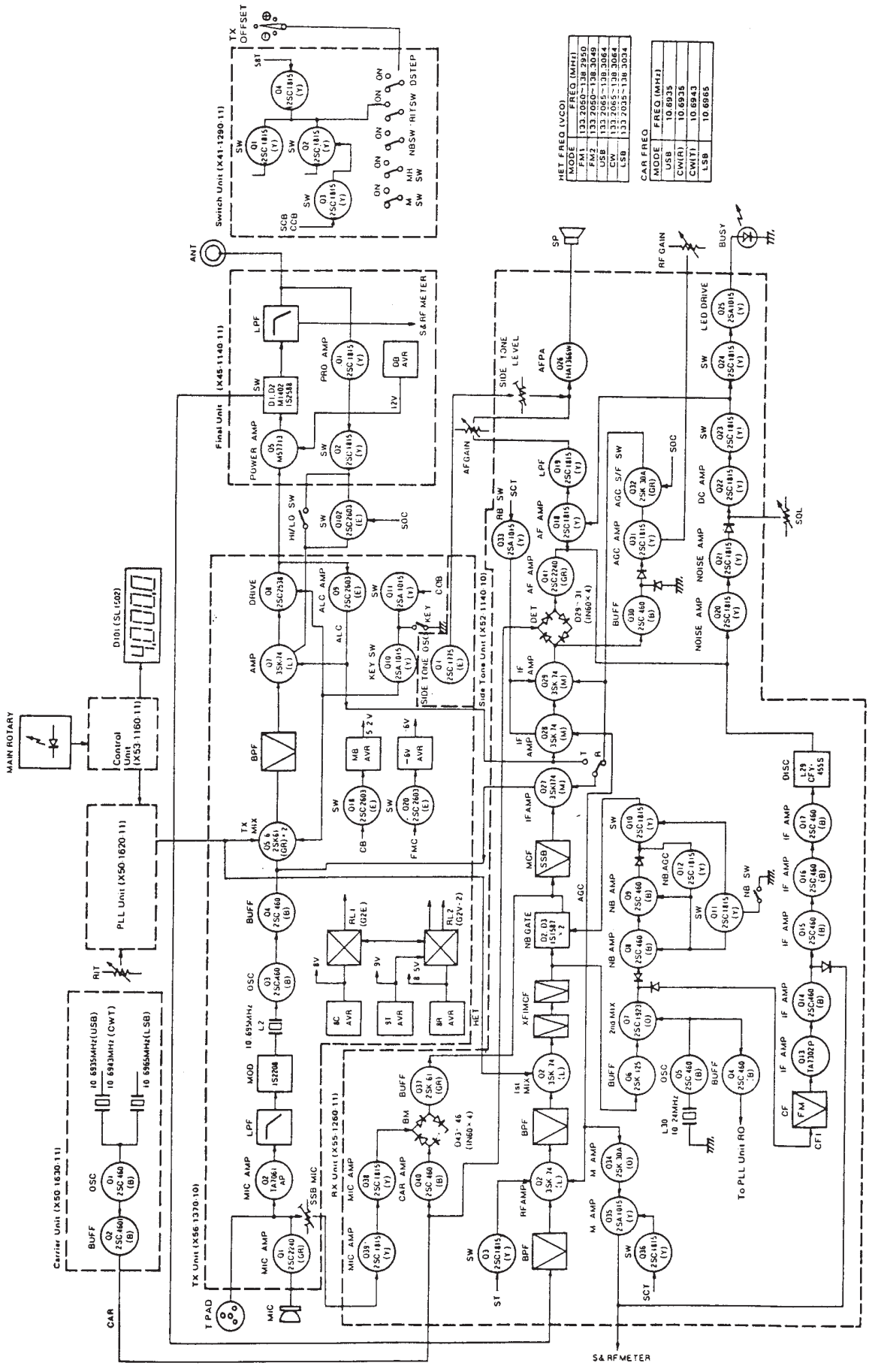
PS-20 BO-9



CONTENTS

2m ALL MODE TRANSCEIVER

BLOCK DIAGRAM (K)



CIRCUIT DESCRIPTION

RX Section

The front end unit is comprised of a dual gate MOS FET and helical resonator. The 2-stage MCF (Monolithic Crystal Filter) following the 1st mixer Q2 (3SK74) provides excellent 2-signal characteristic and high sensitivity.

The IF signal from the MCF is divided and applied to the SSB and FM circuits. The SSB signal passes through the NB (Noise Blanker) gate crystal filter (10H2.2SD) and is amplified by the transmit/receive IF amplifier, Q27, Q28 and 29, and is then demodulated into an audio signal by the product detector.

In the NB circuit, the signal from the MCF passes through the buffer amplifier Q6 and is fed to the 2nd mixer Q7. This signal is converted 455 kHz and the noise is amplified by two stages for switching the NB gate. The NB is front panel controlled.

In the AGC circuit, the signal from the final IF stage is detected and amplified, and the time constant is automatically select according to the mode of operation, FAST in CW mode and SLOW in SSB mode. The AGC signal is applied to the 3-stage IF amplifier, Q27, 28 and 29 (3SK74), and the RF amplifier Q1. The AGC voltage is also used for meter indication.

In the FM circuit, the signal from the ceramic filter CFW-455E is amplified by the IF amplifier Q13 (TA7302P). The auto scan stop signal is applied to the micro-computer from the squelch circuit.

The detected AF signal is amplified by the AF amplifier Q18, a 2SC1815(Y). The amplified signal passes through the LPF (Low Pass Filter) Q19, a 2SC1815(Y) and is power-amplified by Q26, (HA1366W) via the AF GAIN control to drive the speaker.

Item	Symbol	Condition (Ta=25°C)	Rating			Unit
			MIN	TYP	MAX	
DC current with no input	Iq	Vin = 0	—	30.0	60.0	mA
Gain in voltage	Gv	Vin = −50 dB	50.0	52.5	55.0	dB
Output power	Po	THD = 10%	4.5	5.5	—	W
Distortion	THD	Po = 0.5W	—	—	1.5	%
Noise level	WBN	Rg = 10 kΩ, BW=20 Hz ~ 20 kHz	—	—	2.0	mV
Hum ratio	HR	f = 500 Hz	28.0	—	—	dB
Voltage allowance with a shorted load		f = 500 Hz Vin = 10 mV, t = 5 sec.	16.0	—	—	V

Rank	1	2	3
Gv (dB)	50.0 ~ 52.2	51.4 ~ 53.6	52.8 ~ 55.0

Table 1. HA1366W (RX Unit : Q26)

Item	Rating
Nominal center frequency	455 kHz
6 dB bandwidth	±7.5 kHz or more
50 dB bandwidth	±15 kHz or less
Ripple (within 455 ±5 kHz)	3 dB or less
Loss	6 dB or less
Guaranteed attenuation (within 455 ±100 kHz)	35 dB or more
Input and output impedance	1.5 kΩ

Table 2. Ceramic filter (L72-0316-05) CFW455E (RX Unit : CF1)

Item	Rating
Nominal center frequency (fo)	10.695 MHz
Center frequency	Within fo ±200 Hz at 6 dB
Pass bandwidth	2.2 kHz or less at 6 dB
Attenuation bandwidth	±1.5 kHz or less at 20 dB ±2.4 kHz or less at 60 dB
Ripple	Less than 2 dB
Loss	Less than 5 dB
Guaranteed attenuation	60 dB or more within ±40 kHz
Input and output impedance	600Ω ±10%/15 pF ±10%

Table 3. Crystal filter (L71-0215-05) 10H2.2SD (RX Unit : XF2)

Item	Rating
Nominal center frequency (fo)	10.695 MHz
Pass bandwidth	±7.5 kHz or more at 3 dB
Attenuation bandwidth	±25 kHz or less at 40 dB ±45 kHz or less at 60 dB
Guaranteed attenuation	1. 70 dB or more within ±1 MHz 2. Spurious level = 40 dB or more at fo ~ fo + 500 kHz 3. Spurious level = 80 dB or more at fo − (910 kHz ±10 kHz)
Ripple Loss	1.0 dB or less 1.5 dB or less
Impedance	3 kΩ/0 pF

Table 4. MCF (L71-0216-05) (RX Unit : XF1)

TX Section

The microphone signal is amplified by the SSB/FM microphone amplifier Q1, a 2SC2240 (GR). This is then divided and fed to the SSB and FM circuits. SSB signal passes through the MIC GAIN control and is fed to the RX

CIRCUIT DESCRIPTION

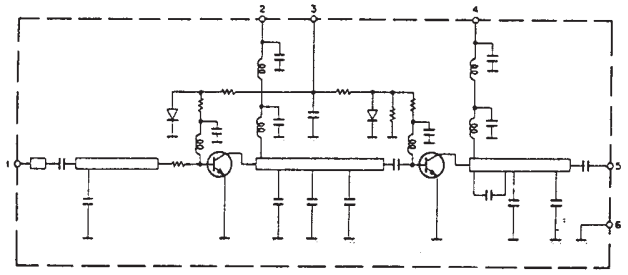
unit where the signal is amplified by two stages and is then applied to the balanced modulator together with the carrier signal (10.695 MHz). The DSB (Double Side Band) signal from the buffer amplifier Q37, a 2SK61 (GR) is fed to the transmit/receive crystal filter to produce an SSB signal. This signal is amplified and applied to the transmit balanced mixer, Q5 and Q6, 2SK61 (GR), in the TX unit. The FM signal is limiter-amplified by Q2 (TA7061AP) and is directly modulated by a 1S2208 diode. The modulated signal is applied to the mixer through the oscillator circuit Q3 (10.695 MHz) and buffer amplifier Q4 a 2SC460 (B). The remaining circuits are common to all the operating modes. The 4-stage BPF (Band Pass Filter) next to the mixer is used to eliminate unwanted spurious signals. After filtering, the signal is amplified by Q7, a 3SK74 (L) to drive the final unit via Q8 (2SC2538).

In the ALC circuit, the drive output from Q8 is amplified by Q9, a 2SC2603 (E) and is applied to the 2nd gates of the predriver Q7 and IF amplifier Q27.

The HI/LOW selection and protection in the FM and CW modes is accomplished by changing the source voltage of Q7, the predriver. In CW mode, the keying circuit controls the transmit balanced mixer B+ line and the base circuit of the predriver Q8 by the switching action of Q10, a 2SC1015 (Y). This signal, fed to the final unit, is power-amplified by the power module (M57713), and is then output to the antenna through, the LPF (Low Pass Filter). The M57713 is designed to provide excellent power, idle current, IMD and "f" characteristics, thus insuring stabilized performance.

Item	Symbol	Tc (°C)	Rating
Operating voltage	Vcc	25	17V
DC current	Icc	25	6A
Operating case temperature	Tc (op)	—	−30 ~ +110°C
Storage temperature	Tstg	—	−40 ~ +110°C
Base bias voltage	VBB	25	10V

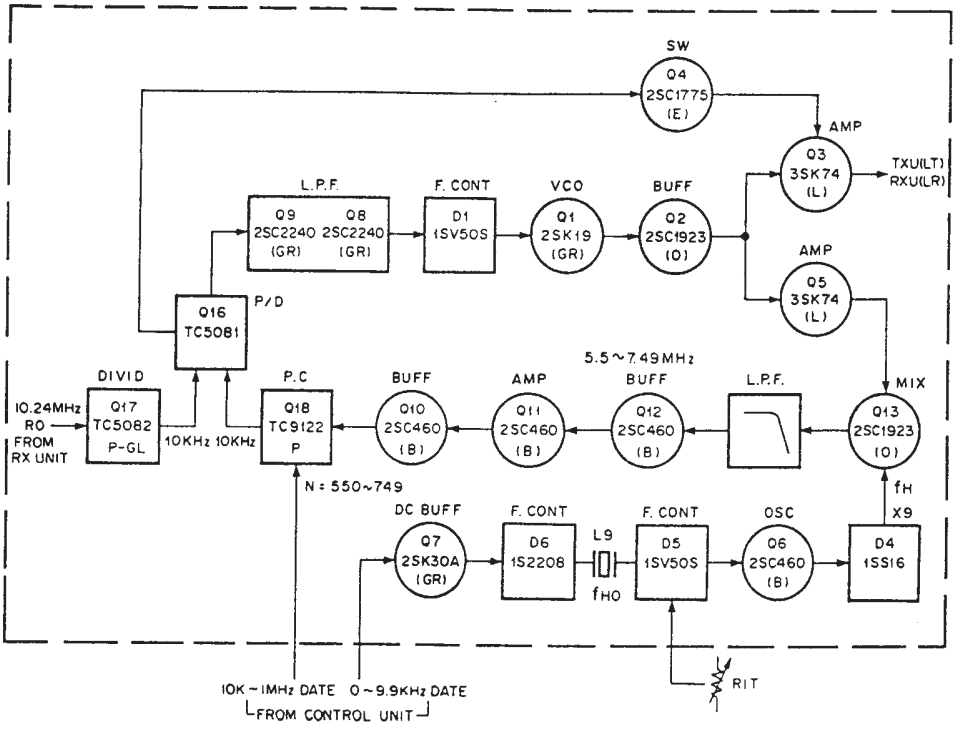
Table 5. Power module (V30-1131-06) M57713 MAX Rating (Final Unit : Q5)



1 : INPUT
2 : Vcc_1
3 : BASE BIAS
4 : Vcc_2
5 : OUT
6 : GND

Fig. 1 Power module (V30-1131-06) Equivalent Circuit

PLL Unit (X50-1620-11)



VCO FREQ

MODE	FREQ (MHz)
FM1	133.305 ~ 135.285
FM2	133.305 ~ 135.3049
USB CW	133.3065 ~ 135.3064
LSB	133.3035 ~ 135.3034

HET OSC FREQ fHO

MODE	FREQ (MHz)
FM1	14.20055
FM2	14.20055 ~ 14.20165
USB CW	14.20072 ~ 14.20182
LSB	14.20039 ~ 14.20149

PLL HET FREQ fH

MODE	FREQ (MHz)
FM1	127.805
FM2	127.805 ~ 127.8149
USB CW	127.8065 ~ 127.8164
LSB	127.8035 ~ 127.8134

Fig. 2 PLL Unit Block Diagram

CIRCUIT DESCRIPTION

PLL Unit (X50-1620-11)

Fig. 2 shows a basic block diagram of PLL circuit. The signal from the VCO (Q1, a 2SK19 (GR)) passes through the buffer amplifier formed by Q2, a 2SC1923 (O) and Q5, a 3SK74 (L), and is then mixed with the HET (Heterodyne) signal by Q13, a 2SC1923 (O) to produce 5.5 ~ 7.49 MHz signal. This signal is amplified by Q10, 11 and Q12, 2SC460 (B) and is frequency-divided by Q18 (TC9122P) according to the BCD data (MHz, 100 kHz and 10 kHz order) from the control unit, to produce 10 kHz comparison signal. Simultaneously, the 10.24 MHz signal from the RX unit is frequency-divided to 1/1024 by Q17 (TC5082P-GL) to produce 10 kHz reference signal. These signals are phase-compared by Q16 (TC5081P) and fed to the LPF formed by Q8 and Q9, and the resulting control voltage is applied to the VCO vari-cap tuning diode.

The 14.2 MHz VCO HET signal is generated by crystal oscillator Q6, a 2SC460 (B), and is then multiplied 9 times by D4 (1SS16) to produce a 127.8 MHz signal. This signal is then applied to the mixer, Q13, a 2SC1923 (O).

The crystal oscillator circuit has two vari-cap diodes to control frequency. A DC signal, corresponding to 0 ~ 9.9 kHz produced by the control unit (X53-1160-00), is voltage converted by Q7, a 2SK30A (GR) and is fed to the vari-cap D6 (1S2208) to control the frequency. The other vari-cap D5 (1SV50S) is used to shift the frequency ($f_{USB} = f_{FM} + 1.5$ kHz, $f_{LSB} = f_{FM} - 1.5$ kHz) according to the operating mode and to afford RIT (Receive Incremental Tuning) frequency.

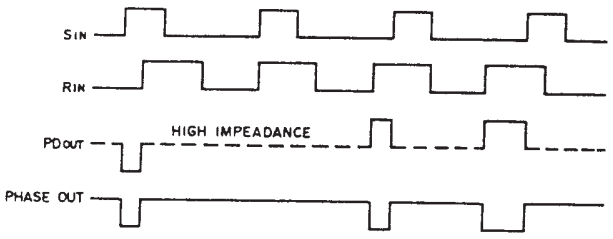


Fig. 3 TC5081P (PLL Unit : Q16)
Phase comparator timing chart

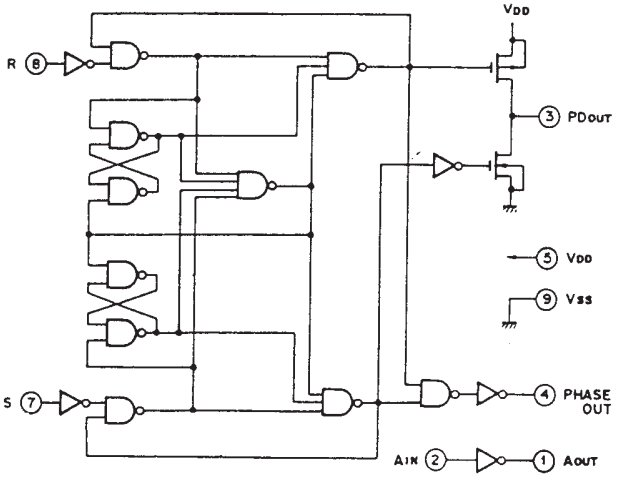


Fig. 4 TC5081P (PLL Unit : Q16)

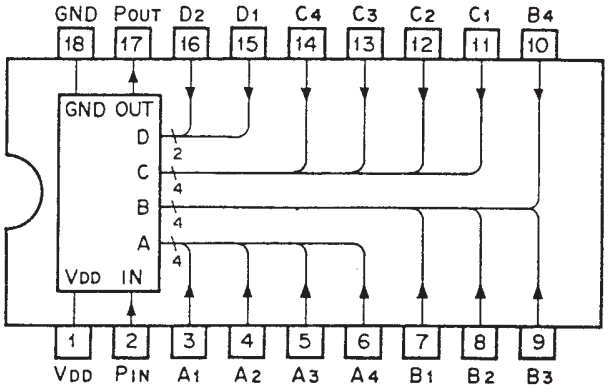


Fig. 5 TC9122P (PLL Unit : Q18)

Symbol	Name	Content and operation	Remarks
Pin	Programmable counter input terminal	Programmable counter input terminal to which the signal to be divided is input.	Build-in bias circuit
Pout	Programmable counter output terminal	Programmable counter output terminal. Output is 1/N of the input frequency. The output pulse width equals 5 bit of the input.	
$A_1 \sim A_4$ $B_1 \sim B_4$ $C_1 \sim C_4$ $D_1 \sim D_2$	× 1 × 10 × 100 × 1000 Program input terminals	Terminal to set the dividing ratio. The following input combination is prohibited.	Built-in pull-down resistor

A_4	A_2	A_1	A_4	B_1	B_2	B_3	B_4	C_1	C_2	C_3	C_4	D_1	D_2
1	0	0	0	0	0	0	0	0	0*	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0

Table 6. Functions of TC 9122P (PLL Unit : Q18)

CONTROL Unit (X53-1160-11)

Fig. 8 shows the basic configuration of control unit. Utilizing the micro-computer to it's full advantage, this control circuit has been designed for a minimum of peripheral control circuits.

- Indicator
  The indicator is a dynamic lighting (scanning) type, using 5-digit LED's. The BCD code data available at the micro-computer D port (pins 8-11) is converted into 7-segment data by the decoder driver Q18 (TC5022BP), so that transistors Q5-9, 2SC1815 (Y) are switched (scanned) in sequence by the digit signal from the E and F ports (pins 12-16) and light the LEDs.
- PLL Data Output
  The PLL MHz, 100 kHz and 10 kHz order data outputs are available directly from the BCD code at the G, H and I ports (pins 22-32). For the 1 kHz and 100 Hz order data, only the indicator data (1 kHz and 100 Hz order) are stored in the dual latch, Q16 (MN1201A) to produce the data for each digit.
  This 2-digit data is converted to a corresponding DC voltage by the D/A converter, a combination of solid resistors (R6-20).
  The MHz, 100 kHz and 10 kHz order data are 550 at 4.00, 650 at 5.00 and 749 at 5.99, respectively (3-digit BCD code).
- Reset Circuit
  The reset circuit is a voltage detecting type. When the source voltage of the micro-computer is increased and exceeds about 3.5V, a current flows into D20, causing Q11,

CIRCUIT DESCRIPTION

a 2SC1815 (Y) to turn ON, which in turn sets the collector of Q10, a 2SC1815 (Y) high, and a reset pulse is input to the micro-computer through the CR differentiation circuit.

- Encoder and UP/DOWN Inputs
  Fig. 7 shows the output signal from the encoder # (50 steps per rotation). This signal is used to discriminate UP and DOWN counts within the micro-computer. The UP count starts when U/D is H level at the down edge of the clock signal, and the DOWN count when U/D is L level.
- Tone Oscillator Circuit
  When the output for the micro-computer tone oscillator is H level, Q12, a 2SC1815 (Y) is energized, allowing a current to flow into the piezo-electric buzzer oscillator, Q13, a 2SC1815 (Y), producing a tone.
- Switching Circuit
  Each of the switches in the control unit are used to select the control pulses output from the micro-computer. Fig. 8 shows a block diagram of the control unit. For actual operation of this unit, the micro-computer input and output terminals must be connected. The diodes (see circuit diagram) are used to prevent control pulses from entering the wrong circuits.

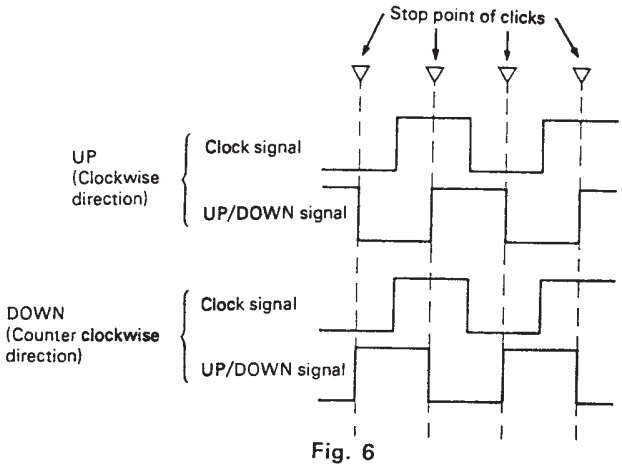


Fig. 6

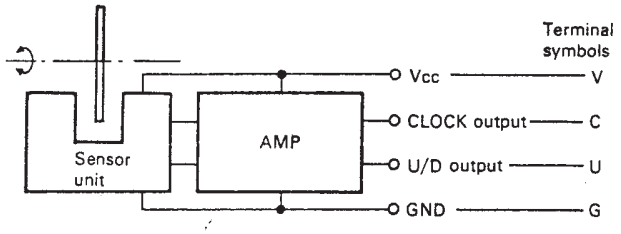


Fig. 7 Rotary encoder (W02-0308-05)

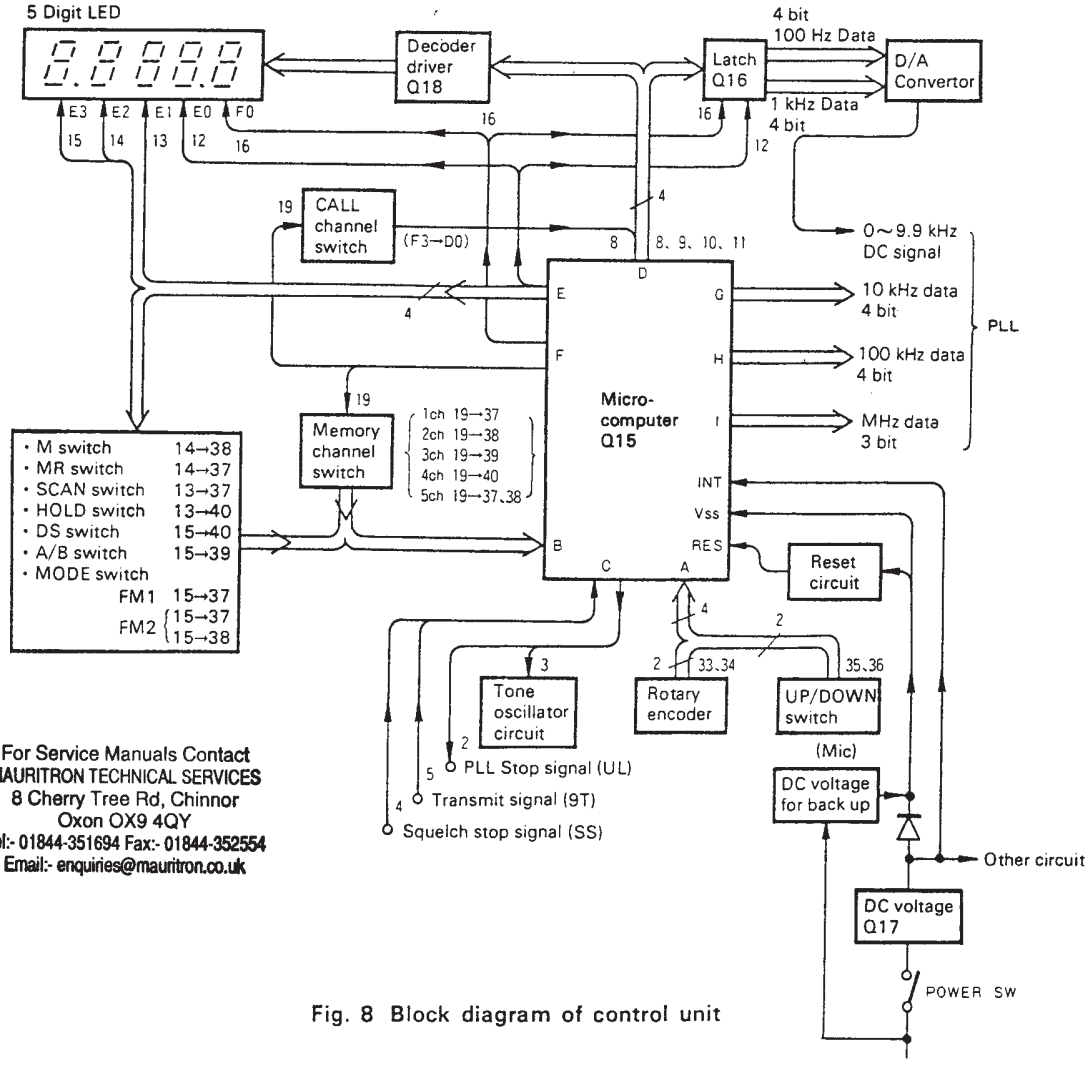


Fig. 8 Block diagram of control unit

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CIRCUIT DESCRIPTION

- Scan Circuit

  This circuit is active when the SCAN switch is depressed. During operation, counting and all other functions are effected within the micro-computer. The scan stops by pressing the HOLD switch or by setting the transmit signal (9T) to H level. The scan stops for a brief period of time when the squelch stop signal (SS terminal) becomes H level. This signal is used to stop the scan in 10 kHz or 20 kHz step. The changes in the 10 kHz PLL data each are differentiated as is or are inverted by Q19, 20 to obtain OR data so that pulses are output each time the data is changed. These pulses are applied to the micro-computer scan stop terminal (4) to slow down the scan operation.

- Control Power Circuit

  The indicator operates on 5V available at transistor Q14, a 2SC496 (Y). The micro-computer operates on 6V supplied by the AVR (Automatic Voltage Regulator) IC, Q17 (NJM78L06K), supplied through a reverse current blocking diode, D11.

- Backup Circuit

  When the POWER SW is turned OFF, the micro-computer operates from the backup power source when the micro-computer INT terminal (pin 6) is at L level. At this time, all

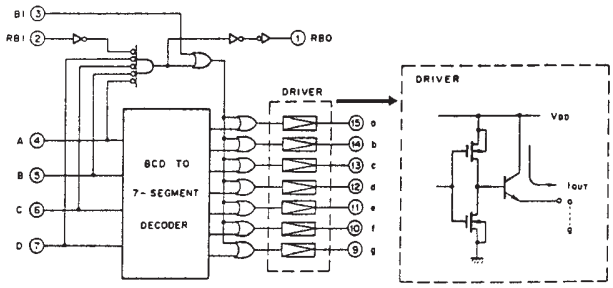

Fig. 9 TC5022BP (Control unit : Q18)

INPUT						OUTPUT							
BI	RBI	A	B	C	D	a	b	c	d	e	f	g	
H	*	*	*	*	*	L	L	L	L	L	L	L	☆
L	H	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	H	H	H	H	H	L	L
L	*	H	L	L	L	L	H	H	L	L	L	L	L
L	*	L	H	L	L	H	H	L	H	H	L	H	L
L	*	H	H	L	L	H	H	H	H	L	L	H	L
L	*	L	L	H	L	L	H	H	L	L	H	H	L
L	*	H	L	H	L	H	L	H	H	L	H	H	L
L	*	L	H	H	L	H	L	H	H	H	H	H	L
L	*	H	H	H	L	H	H	H	L	L	H	L	L
L	*	L	L	L	H	H	H	H	H	H	H	H	L
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L	*	H	H	L	H	L	H	H	L	L	L	L	L
L	*	L	L	H	H	H	H	L	H	H	L	H	L
L	*	H	L	H	H	H	H	H	L	L	H	H	L
L	*	L	H	H	H	L	H	H	H	L	H	H	L
L	*	H	H	H	H	H	L	H	H	L	H	H	L

Table 8 Truth table of TC5022BP (Control unit : Q18)

☆ : Undetermined
* : Don't Care

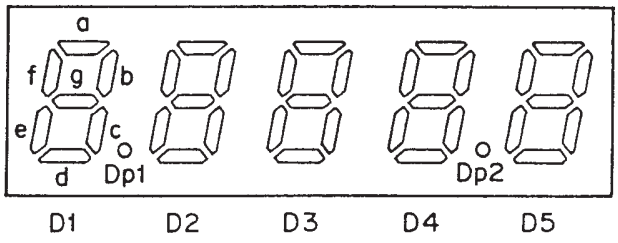
Pin No.	Pin	Input signal	Output signal	Description	Pulse
1	CL1			Clock signal 400 kHz	
2	PC0	O		Normally L, H at prohibited transmitting	
3	PC1	O		Normally L, H at Tone ON	
4	PC2	O		Squelch signal, H at Busy stop	
5	PC3	O		Normally L, H at transmit	
6	INT	O		Normally H	
7	RES	O		H at reset	
8	PD0	O	O	Call channel input signal. 100 Hz, 1 kHz order data output.	O
9	PD1		O		O
10	PD2		O		O
11	PD3		O		O
12	PE0		O	1 kHz order data output, latch pulse	O
13	PE1		O	10 kHz order data output SCAN, HOLD output	O
14	PE2		O	100 kHz order data output M, MR output	O
15	PE3		O	1 MHz order data output DS, A/B, MODE output	O
16	PF0		O	100 Hz order data output Latch pulse	O
17	PF1		O	Not used (open)	
18	PF2		O	Not used (open)	
19	PF3		O	CALL, MEMORY output	O
20	TEST	O		Normally H	
21	Vcc	O		5V DC supply	

Pin No.	Pin	Input signal	Output signal	Description	Pulse
22	PG0		O	A	
23	PG1		O	B — 10 kHz order data output for PLL	
24	PG2		O	C	
25	PG3		O	D	
26	PH0		O	A	
27	PH1		O	B — 100 kHz order data output for PLL	
28	PH2		O	C	
29	PH3		O	D	
30	PI0		O	A	
31	PI1		O	B — MHz order data output for PLL	
32	PI2		O	C	
33	PA0	O		Encoder input, clock	
34	PA1	O		Encoder input, UP/DOWN	
35	PA2	O		Normally H, L at MIC UP operation	
36	PA3	O		Normally H, L at MIC DOWN operation	
37	PB0	O		MR, SCAN, MODE-FM1, MEMORY 1, 5CH pulse input	O
38	PB1	O		M, MODE-FM2, MEMORY 2, 5CH pulse input	O
39	PB2	O		VFO-B, MEMORY 3CH pulse input	O
40	PB3	O		SEARCH, MEMORY, 4CH pulse input	O
41	Vss			Grounded	
42	CLO			Clock signal 400 kHz	

Table 7. Functions of μPD650C-021 (Control Unit: Q15)

CIRCUIT DESCRIPTION

output ports become L level, minimizing power consumption. When the POWER SW is turned ON, the INT terminal and UP/DOWN input terminal become H level, and the micro-computer resumes at its original condition. The input port B (pins 37-40) is momentarily set to L level by Q2 and Q4 to insure backup operation even when other switches remain ON. Backup operation is also assured during scan operation, since the scan is stopped by Q3 when the POWER SW is turned OFF.



Symbol	Pin	Description
IN1 ~ IN4	Input	4-bit input terminal
AO1 ~ AO4	Output	Output terminal for data latched by clock pulse CKA
BO1 ~ BO4	Output	Output terminal for data latched by clock pulse CKB
CKA	Clock A	Clock signal terminal for latching 4-bit input signal in 4-bit flip flop A. Input signal is latched at the rising of clock signal.
CKB	Clock B	Clock signal terminal for latching 4-bit input signal in 4-bit flip flop B. Input signal is latched at the rising of clock signal.

Table 9. Function of MN 1201A (Control Unit : Q16)

Pin No.	Address	Pin No.	Address
1	D5, Dp2 Cathode	9	e Anode
2	D4 Cathode	10	d Anode
3	D3 Cathode	11	c Anode
4	D2 Cathode	12	g Anode
5	D1, Dp1 Cathode	13	b Anode
6	Open	14	a Anode
7	Dp1, Dp2 Anode	15	f Anode
8	Dp1, Dp2 Anode		

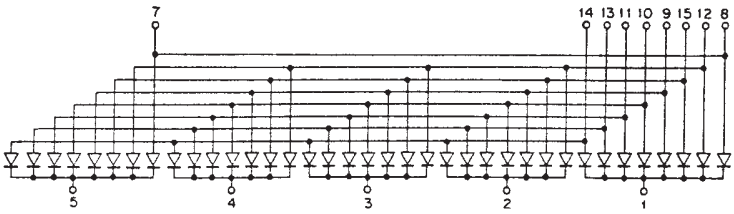


Fig. 11 5 digit LED D101 : SL1502

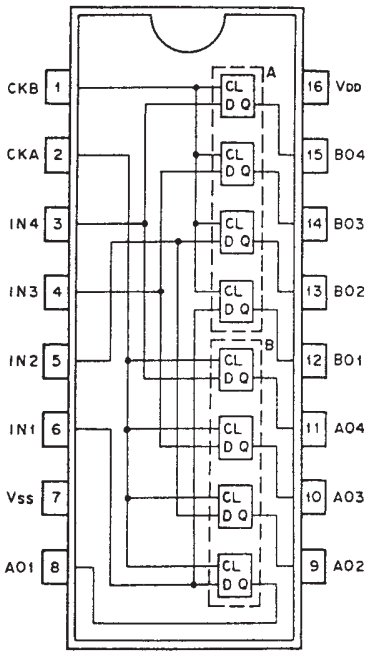
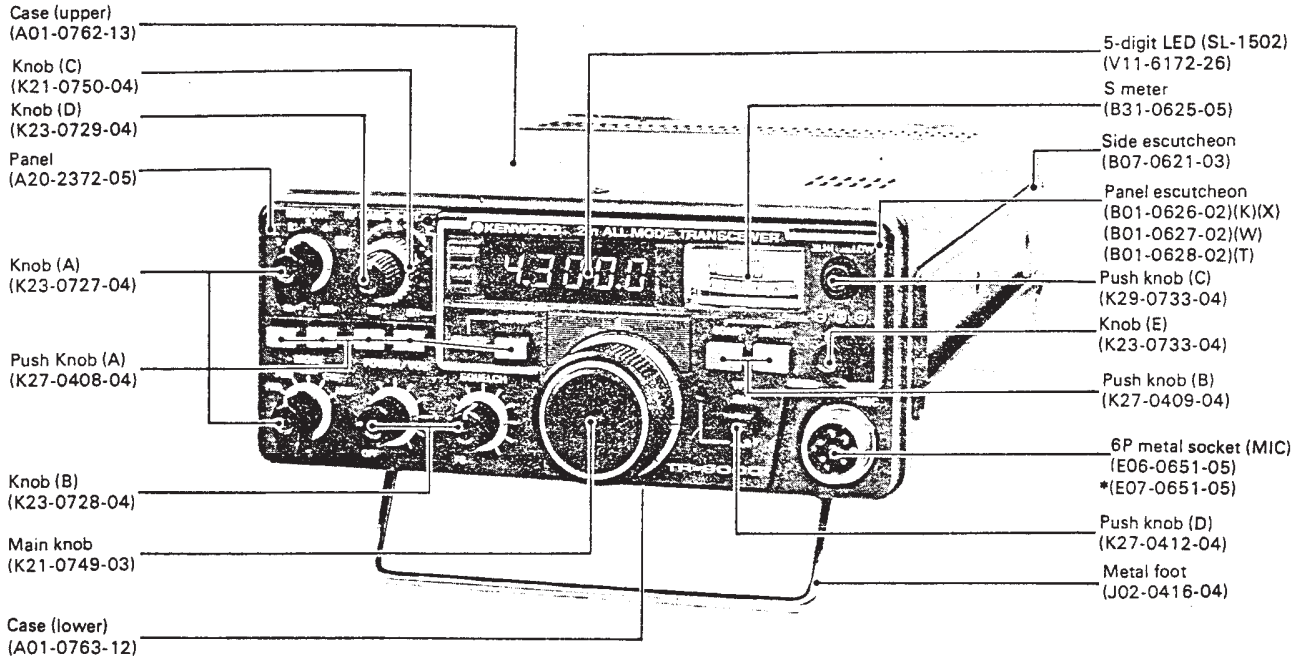


Fig. 10 MN1201A (Control unit : Q16)

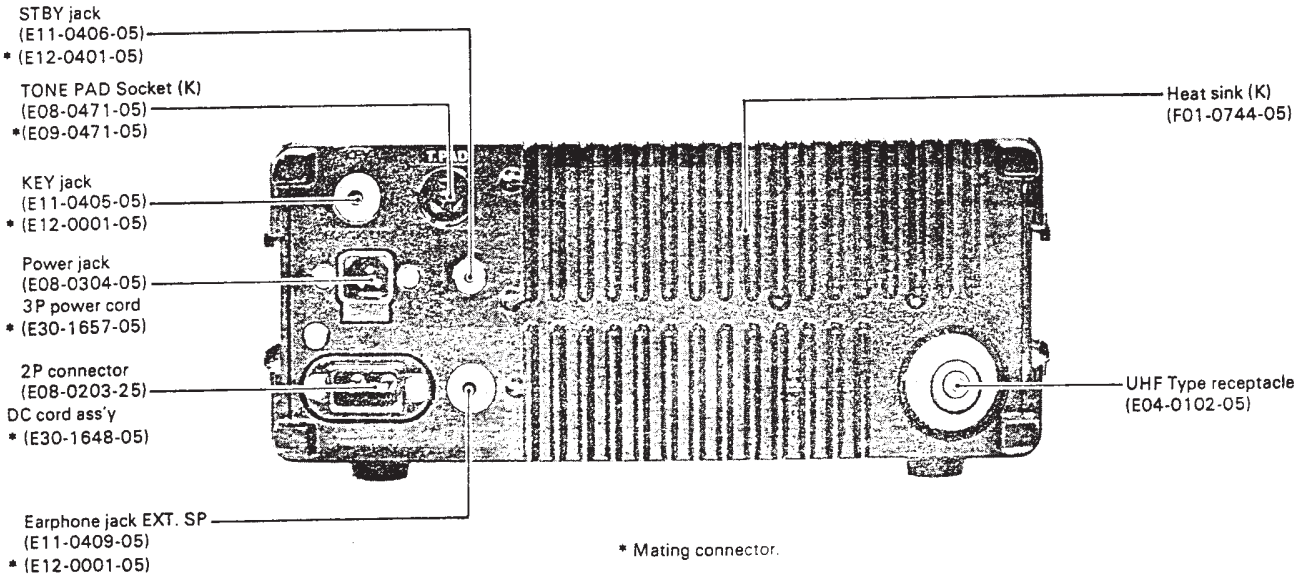
OUTSIDE VIEWS

<FRONT PANEL> TR-9000 (K)



* Mating connector

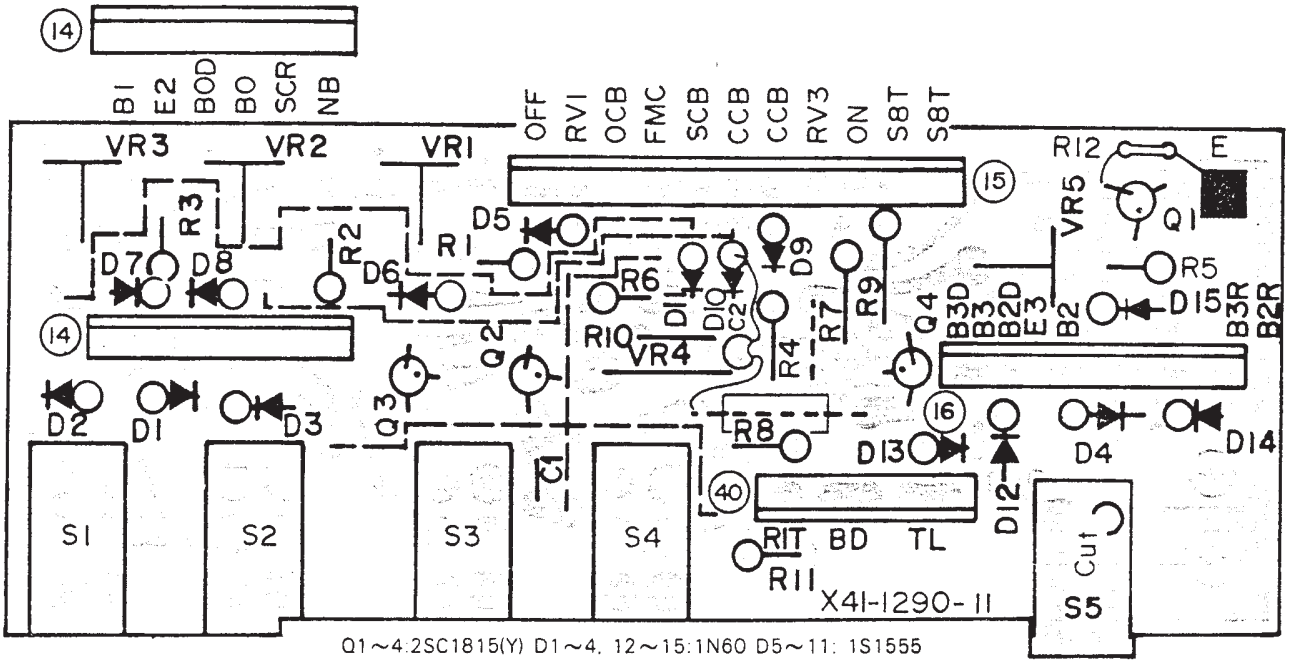
<REAR PANEL> TR-9000 (K)



* Mating connector.

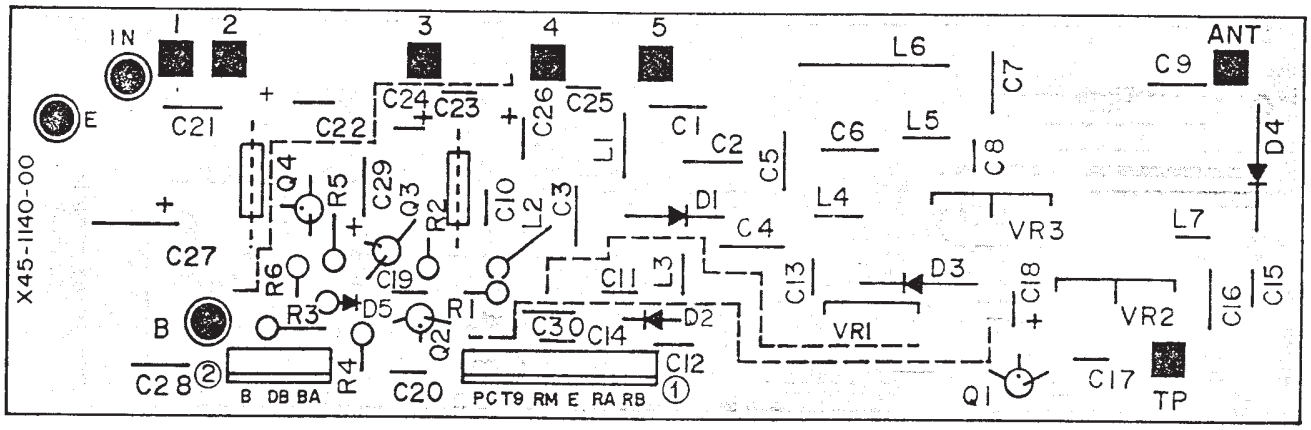
PC BOARD VIEWS

▼ SWITCH UNIT (X41-1290-11) PARTS LIST: Page 19



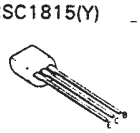
Q1～4:2SC1815(Y) D1～4, 12～15:1N60 D5～11: 1S1555

▼ FINAL UNIT (X45-1140-00) (W)(T)(X) PARTS LIST: Page 20
(X45-1140-11) (K)

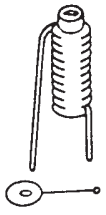


Q1,2,4:2SC1815(Y) Q3:2SA1015(Y) Q5:M57713 D1:MI402 D2:1S2588 D3,4:1N60 D5:1S1555 D6:U05B

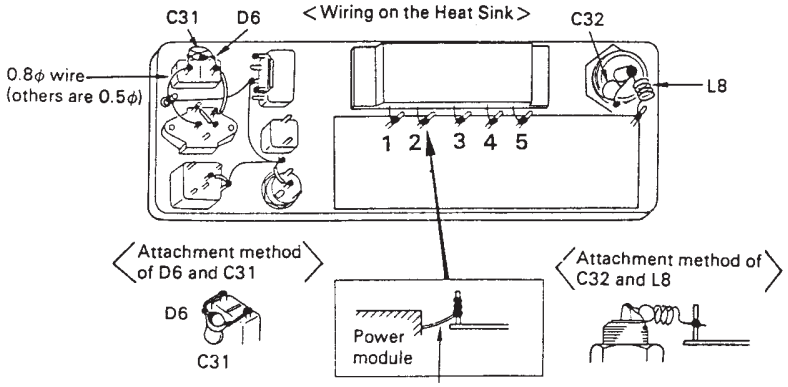
2SA1015(Y)
2SC1815(Y)



<Attachment direction of L2>

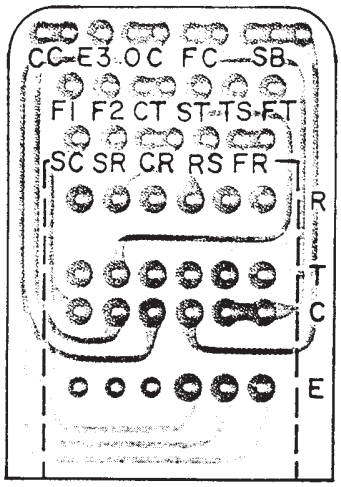


<Wiring on the Heat Sink>

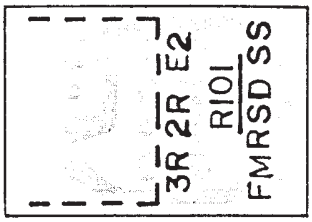


PC BOARD VIEWS

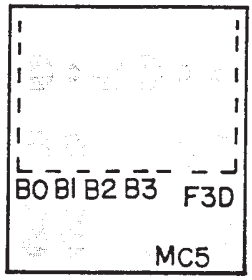
▼ MODE (J25-2714-04)



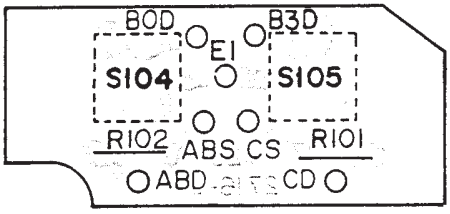
▼ TX OFF SET (J25-2744-04)



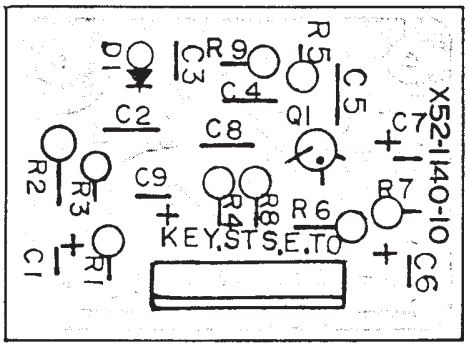
▼ MEMORY (J25-2715-04)



▼ SCAN (J25-2716-24)



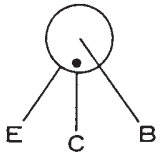
▼ SIDE TONE UNIT (X52-1140-10)
PARTS LIST: Page 21



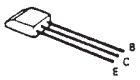
Q1: 2SC1775(E) D1: 1S1555

NOTES:
All printed circuit views are component side.

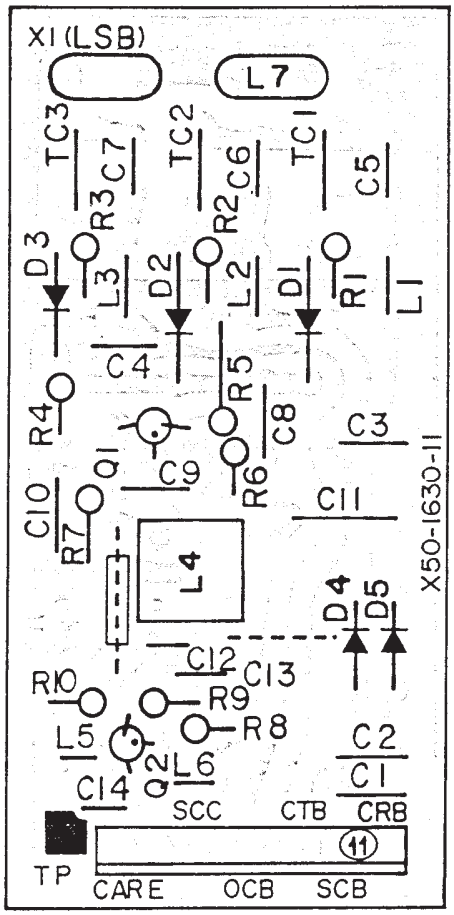
[Transistor Terminal Indication]



2SC460(B)



▼ CAR UNIT (X50-1630-11)
PARTS LIST: Page 21

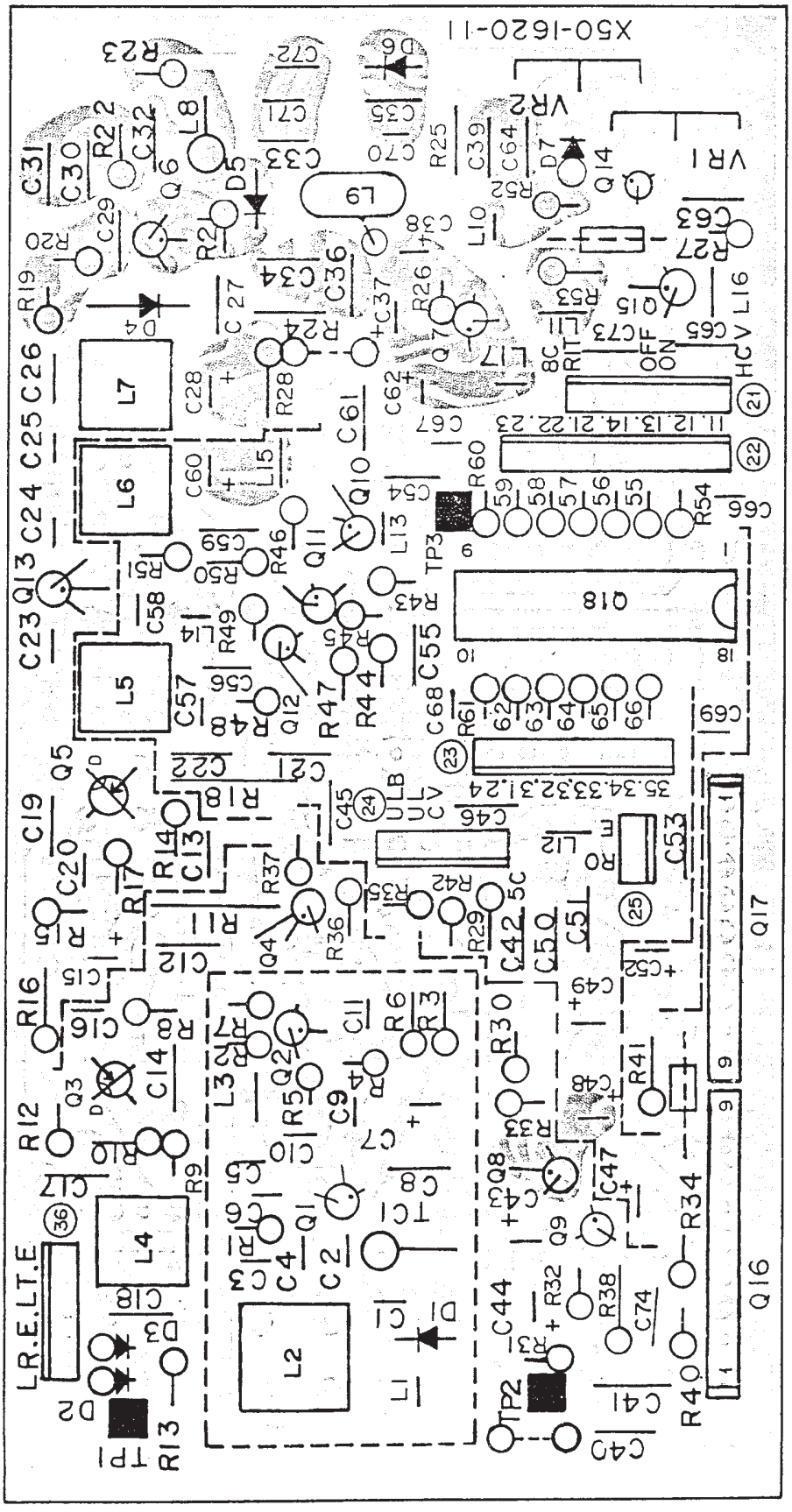


Q1, 2.2SC460(B) D1~5:1S1555

PC BOARD VIEW

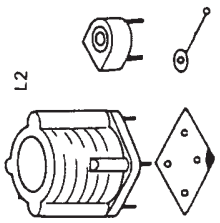
For Service Manuals Contact
MAURITRON TECHNICAL SERVICES
8 Cherry Tree Rd, Chinnor
Oxon OX9 4QY
Tel:- 01844-351694 Fax:- 01844-352554
Email:- enquiries@mauritron.co.uk

▲ PLL UNIT (X50-1620-00)(W)(T) (X50-1620-11)(K)(X)

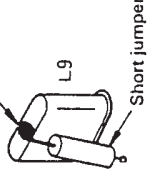


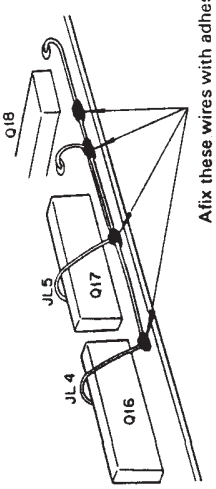
Q1,2:2SK19(GR) Q2,13:2SC1923(O) Q3,5:3SK74(L) Q4:2SC1775(E) Q6,10~12:2SC460(B) Q7:2SK30A(GR) Q8,9:2SC2240(GR)
Q14,15:2SC1815(Y) Q16:TC5081P Q17:TC5082P-GL Q18:TC9122P
D1,5:1SV50S D2,3:1S2588 D4:1SS16 D6:1S2208 D7:1S1555

< Attachment direction of TC1 and L2 >



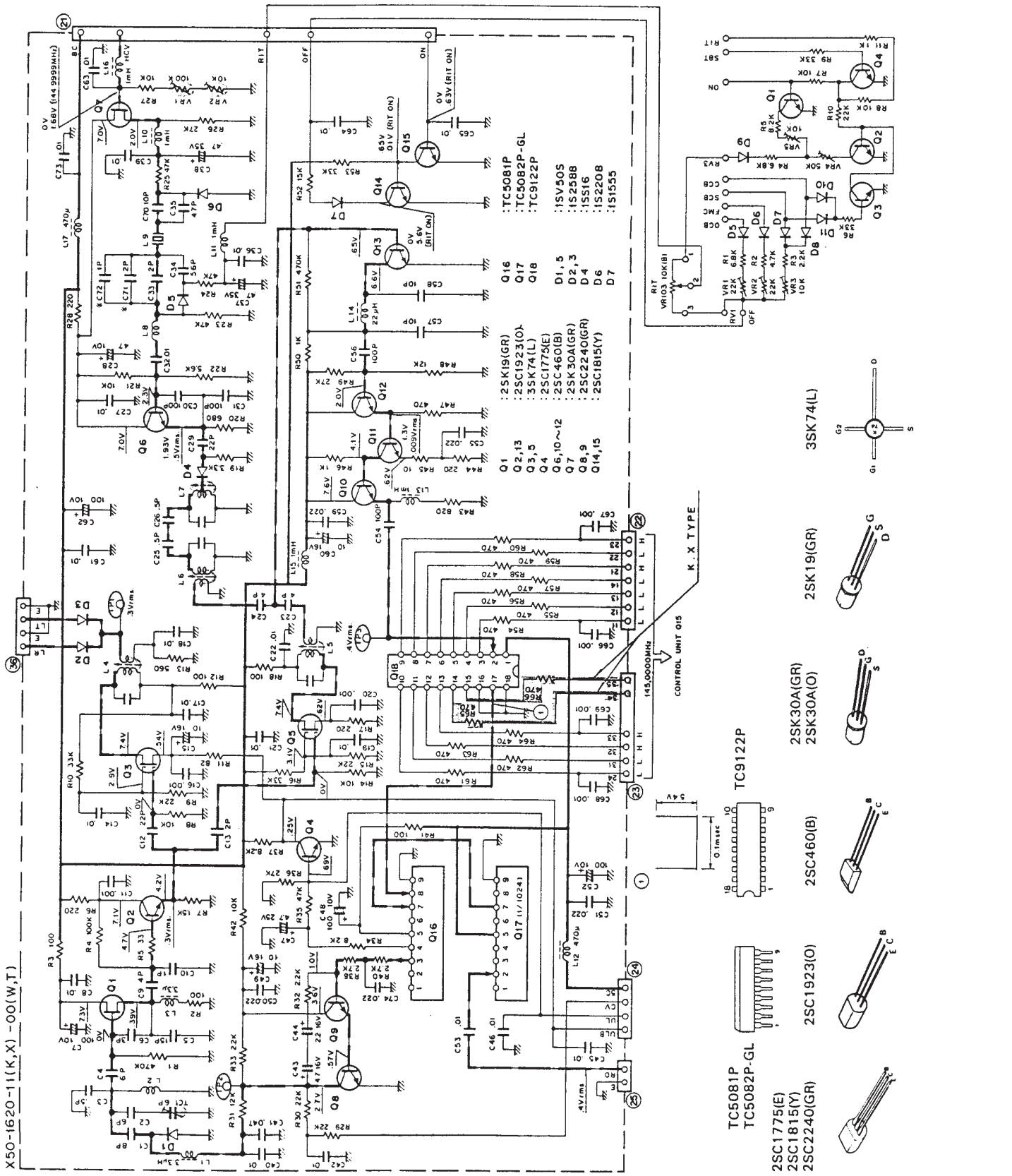
< Attachment method of L9 >





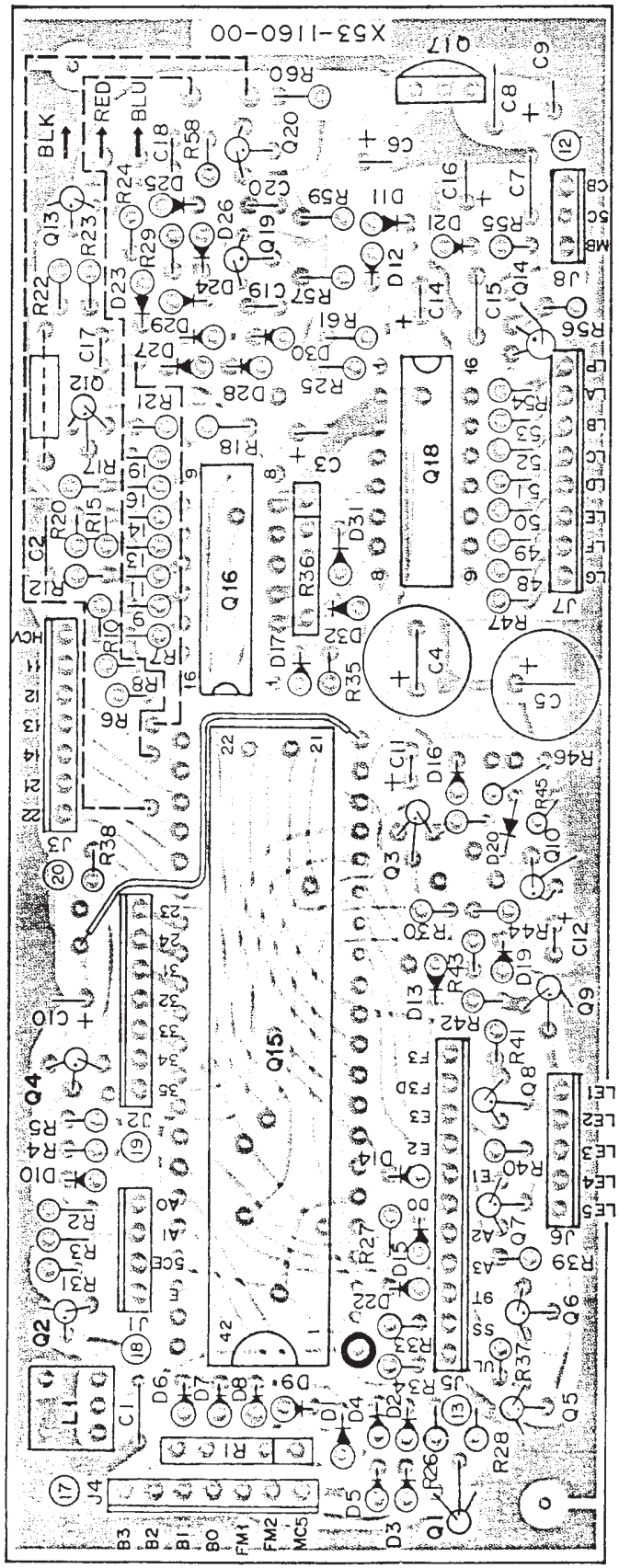
CIRCUIT DIAGRAM

▼ PLL Unit (X50-1620-00)(W)(T) (X50-1620-11)(K)(X) PARTS LIST: Page 20



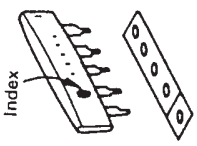
PC BOARD VIEW

▼ CONTROL UNIT (X53-1160-11) (K) (X53-1160-61 (W)(T) (X53-1160-71) (X)

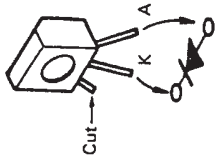


Q1,2,5~13,19,20:2SC1815(Y) Q3,4:2SA1015(Y) Q14:2SC496(Y) Q15:μPD650C-021 Q16:MN1201A
Q17:NJM78L06K Q18:TC5022BP D1,13,14,17,22~32:1N60 D2~12,15,16,19:1S1555
D20:MA522(Q) D21:XZ-057

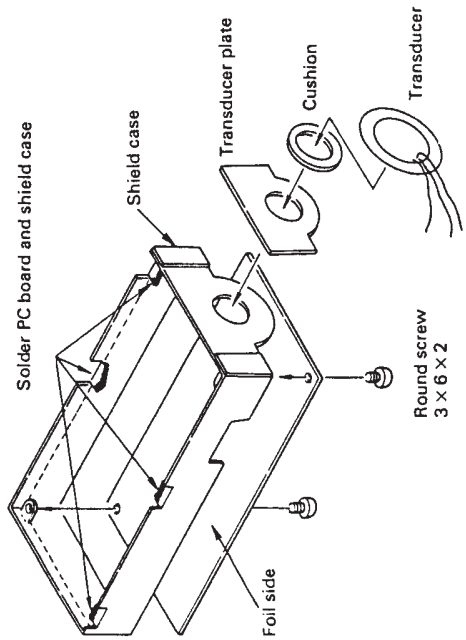
<Attachment direction of R1 and R36>



<Attachment direction of D20>



<Attachment method of the shield case and Tone transducer>



CIRCUIT DIAGRAM

▼ CONTROL UNIT (X53-1160-11) (K) (X53-1160-61) (W)(T) (X53-1160-71)(X)

PARTS LIST: Page 22